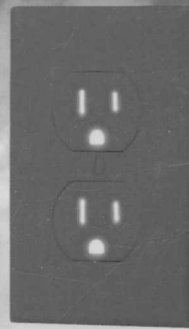
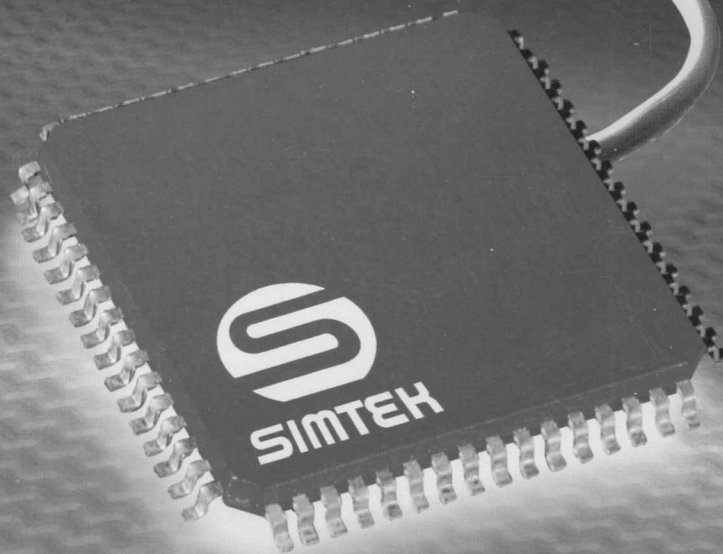


1995 nvSRAM DATA BOOK



SIMTEK





SIMTEK

1995 Data Book

Simtek Corporation

1465 Kelly Johnson Boulevard
Colorado Springs, Colorado 80920 USA
800/637-1667; 719/531-9444
Fax: 719/531-9481

Internet Home Page: <http://simtek.com> OR <http://www.csn.net/simtek>

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SIMTEK January 1995 Data Book

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Introduction 1

Simtek Corporation

Our Vision

To be the undisputed world leader in nonvolatile SRAM products & technology, delivering exciting products to the market which simply outpace the competition.

Our Company

Headquartered in Colorado Springs, Colorado, Simtek Corporation was born in 1987. Dr. Richard Petritz, founder of memory companies Inmos and Mostek, formed Simtek along with Dr. Gary Derbenwick. Strategic alliances have allowed Simtek to reduce capital requirements, as well as having access to leading-edge facilities. Currently, Simtek subcontracts all phases of the manufacturing process.

Our Products

Simtek has taken the most desired features of volatile and nonvolatile memory, and combined them into a single chip: the nvSRAM.

The nvSRAM combines static random access memory (SRAM) and electrically eraseable programmable read-only memory (EEPROM) in a shadow memory configuration. Within each SRAM cell is an additional EEPROM cell, which can be read directly to (or written from) the external data pins, in a manner identical to conventional SRAM operation.

Achieving Standard Military Drawings from the government, Simtek's nvSRAMs answer the needs of high end military systems, as well as meeting cost requirements to be the ideal solution for volume commercial products. A sampling of applications ideal for Simtek's family of nvSRAM products include: cellular telephones, high density hard disk drives, modems, smart utility meters, home and commercial security systems, instrumentation, and numerous military systems including communications, radar, sonar and smart weapons.

Using Simtek's proprietary NOVCEL™ technology, Simtek's 256 kilobit nvSRAM product family currently has sixteen times the density of its closest competitive single-chip NVSRAM. With access times to 25 nanoseconds, Simtek's nvSRAM performs as quickly as industry standard SRAMs.

Our Future

NOVCEL™ technology offers Simtek the path to even higher densities (Meg and beyond) and submicron die sizes. This path provides accelerated product development, cost reduction, and a baseline for products combining logic, RAM and NOVCEL based memory on the same chip.

Simtek will continue to pursue strategic alliances in all aspects of business.

Simtek Data Sheets

Advance Data Sheets

Advance datasheets include information on products in early design stage.

Preliminary Data Sheets

Data sheets marked "Preliminary" are planned for full production availability in the near future. Typically, samples of devices covered by preliminary data sheets are available.

Final Data Sheets

Unmarked with preliminary or advanced, "Final" data sheets cover fully qualified devices available in production quantities.

Simtek Product

Engineering Samples

Units shipped as "Engineering Samples" are provided to selected customers for preliminary device evaluation. These units will be marked "ENG" on the top of the package. These devices may not be fully functional and may not have been fully characterized, tested or burned-in. Engineering Samples will not have been submitted to formal qualification testing. Simtek does not guarantee the functionality or reliability of these units.

Sample

Marked "Sample", these devices are units which are from qualified design/process revisions which have not been tested to the full production flow. Topside marking will be "SAMPLE" to distinguish the product from normal finished goods devices. Simtek does not guarantee the reliability or functionality of the product.

Pre-Qual

Devices which have passed the normal production screening tests, but which have not yet completed formal qualification testing may be shipped to selected customers marked "PRE-QUAL". Most of the formal device characterization will have been completed, and the product will normally be representative of fully qualified production material. Simtek makes no guarantee with respect to the reliability of the product.

Full Production

Units which have passed all production screens, and have met Simtek's reliability standards, will be released as fully qualified product. Such devices will meet the specifications listed in the Final Data Sheet, and the published Simtek quality and reliability standards.

Simtek reserves the right to make any changes without notice.

Questions?

Please call! (800) 637-1667 OR (719) 531-9444



Simtek nvSRAM Cross Reference Guide

SIMTEK P/N	DESCRIPTION	SIMTEK PACKAGE OPTIONS	COMPETITOR P/N	COMPETITOR PACKAGES
STK20C04	512 x 8	28 pin 600-mil DIP	Xicor: X20C04	28 pin 600-mil DIP 32 pin PLCC 32 pin LCC
STK10C48 STK11C48	2K x 8 Hardware or Software Initiated Store	28 pin 350-mil SOIC 28 pin 300-mil DIP 28 pin 600-mil DIP	Xicor: X2016	28 pin 600-mil DIP 32 pin PLCC 32 pin LCC
STK22C48	2K x 8 AutoStore™	28 pin 600-mil DIP	Xicor: X20C17 Dallas: DS1220 Benchmark: BQ4010 SGS: MK48Z02	24 pin 600-mil DIP 24 pin 600-mil DIP 28 pin 600-mil DIP 24 pin 600-mil DIP
STK25C48	2K x 8 AutoStore™	24 pin 600-mil DIP	Xicor: X20C17 Dallas: DS1220	24 pin 600-mil DIP 24 pin 600-mil DIP
STK10C68 STK11C68	8K x 8 Hardware or Software Initiated Store	28 pin 350-mil SOIC 28 pin 300-mil DIP 28 pin LCC	Xicor: X20C64 Dallas: DS1225 Benchmark: BQ4010 SGS: MK48Z08	28 pin 600-mil DIP 28 pin 600-mil DIP 28 pin 600-mil DIP 28 pin 600-mil DIP
STK12C68	8K x 8 AutoStore™	28 pin 350-mil SOIC 28 pin 300-mil DIP 28 pin 600-mil DIP 28 pin LCC	Xicor: X20C64 Dallas: DS1225 Benchmark: BQ4010 SGS: MK48Z08	28 pin 600-mil DIP 28 pin 600-mil DIP 28 pin 600-mil DIP 28 pin 600-mil DIP
STK11C88	32K x 8 Software Initiated Store	28 pin 600-mil DIP	Dallas: DS1230 Benchmark: BQ4011 SGS: MK48Z32	28 pin 600-mil DIP 28 pin 600-mil DIP 28 pin 600-mil DIP
STK15C88	32K x 8 AutoStore™	28 pin 600-mil DIP	Dallas: DS1230 Benchmark: BQ4011 SGS: MK48Z32	28 pin 600-mil DIP 28 pin 600-mil DIP 28 pin 600-mil DIP
STK12C88	32K x 8 AutoStore™	64 pin QFP 40 pin 600-mil DIP	NONE	N/A
STK12C816	16K x 16 AutoStore™	64 pin QFP	NONE	N/A

4 kilobit nvSRAM Products 2



STK20C04

CMOS nvSRAM

High Performance

512 x 8 Nonvolatile Static RAM

2

FEATURES

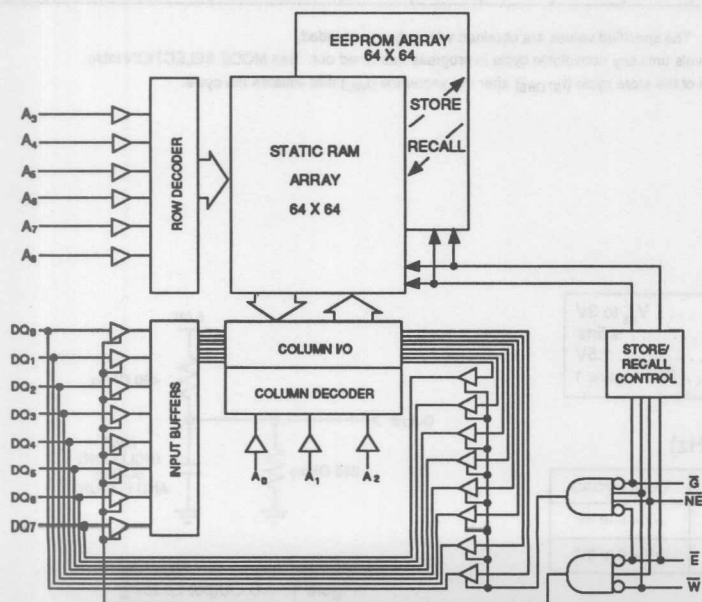
- 30, 35 and 45ns Access Times
- 15, 20 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Hardware *STORE* Initiation
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Hardware *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single 5V±10% Operation
- Commercial and Industrial Temperatures
- Available in 600 mil PDIP package

DESCRIPTION

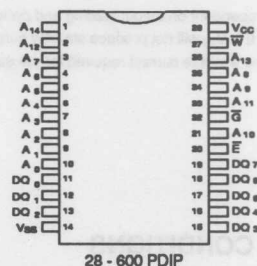
The Simtek STK20C04 is a fast static RAM (30, 35, 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) using the $\overline{NE}$ pin. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

The STK20C04 features the industry standard pinout for nonvolatile RAMs in a 28-pin 600 mil plastic DIP.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A ₀ - A ₈	Address Inputs
W	Write Enable
DQ ₀ - DQ ₇	Data In/Out
E	Chip Enable
$\overline{G}$	Output Enable
NE	Nonvolatile Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS}-0.6V to 7.0V
Voltage on $DQ_{0,7}$ and $\bar{Q}$-0.5V to ($V_{CC}+0.5V$)
Temperature under bias.....-55°C to 125°C
Storage temperature.....-65°C to 150°C
Power dissipation.....1W
DC output current.....15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		85		90	mA	$t_{AVAV} = 30ns$
			80		85	mA	$t_{AVAV} = 35ns$
			75		80	mA	$t_{AVAV} = 45ns$
I_{CC2}^d	Average V_{CC} Current during <i>STORE</i> cycle		50		50	mA	All inputs at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		27		30	mA	$t_{AVAV} = 30ns$
			23		27	mA	$t_{AVAV} = 35ns$
			20		23	mA	$t_{AVAV} = 45ns$ $E \geq V_{IH}$; all others cycling
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		1		1	mA	$E \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5		± 5	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+.5$	2.2	$V_{CC}+.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-.5$	0.8	$V_{SS}-.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $E \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note d: I_{CC2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels..... V_{SS} to 3V
Input Rise and Fall Times..... $\leq 5ns$
Input and Output Timing Reference Levels..... 1.5V
Output Load..... See Figure 1

CAPACITANCE^e ($T_A=25^\circ C$, $f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance & W	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

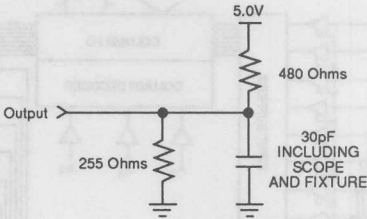


Figure 1: AC Output Loading

READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK20C04-30		STK20C04-35		STK20C04-45		UNITS
	#1, #2	AIL		MIN	MAX	MIN	MAX	MIN	MAX	
1	t _{ELOV}	t _{ACS}	Chip Enable Access Time		30		35		45	ns
2	t _{AVAV} ^g	t _{RC}	Read Cycle Time	30		35		45		ns
3	t _{AVOV} ^h	t _{AA}	Address Access Time		30		35		45	ns
4	t _{GLOV}	t _{OE}	Output Enable to Data Valid		15		20		25	ns
5	t _{AXOX}	t _{OH}	Output Hold After Address Change	5		5		5		ns
6	t _{ELOX}	t _{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t _{EHQZ} ⁱ	t _{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t _{GLOX}	t _{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t _{GHOZ} ⁱ	t _{OHZ}	Output Disable to Output Inactive		15		17		20	ns
10	t _{ELICCH} ^e	t _{PA}	Chip Enable to Power Active	0		0		0		ns
11	t _{EHICCL} ^{c,e}	t _{PS}	Chip Disable to Power Standby		30		35		45	ns
11A	t _{WQOV}	t _{WR}	Write Recovery Time		35		45		55	ns

Note c: Bringing $\bar{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note e: Parameter guaranteed but not tested.

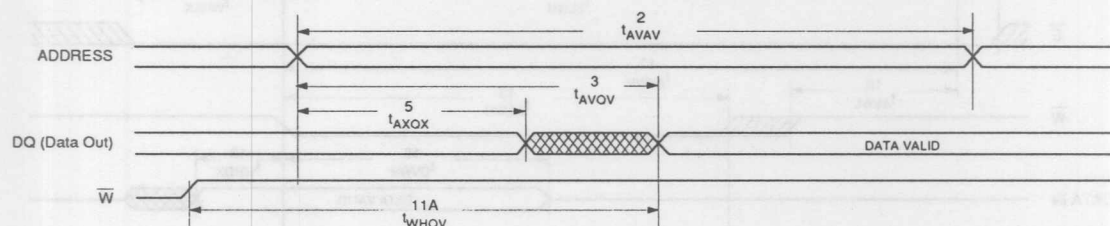
Note f: $\bar{NE}$ must be high during entire cycle.

Note g: For READ CYCLE #1 and #2, $\bar{W}$ and $\bar{NE}$ must be high for entire cycle.

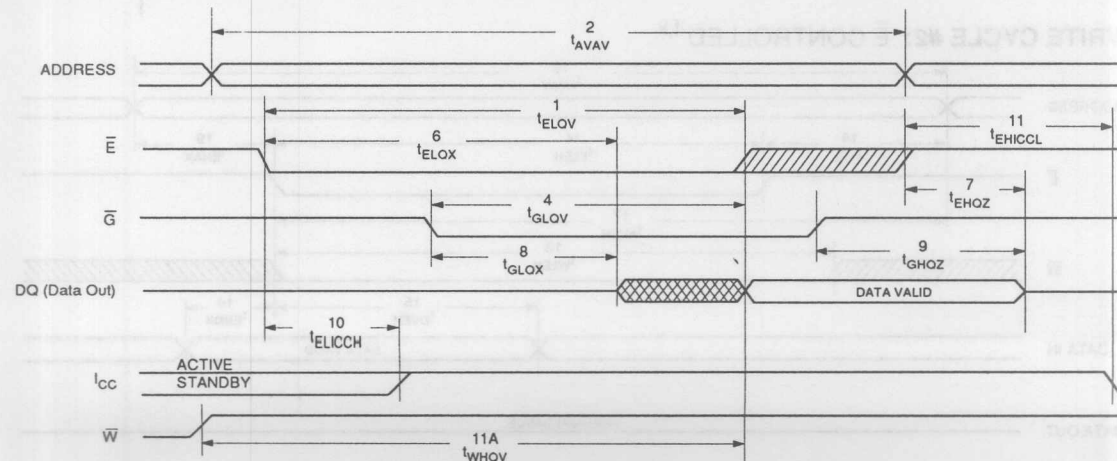
Note h: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note i: Measured ± 200mV from steady state output voltage.

READ CYCLE #1 f,g,h



READ CYCLE #2 f,g



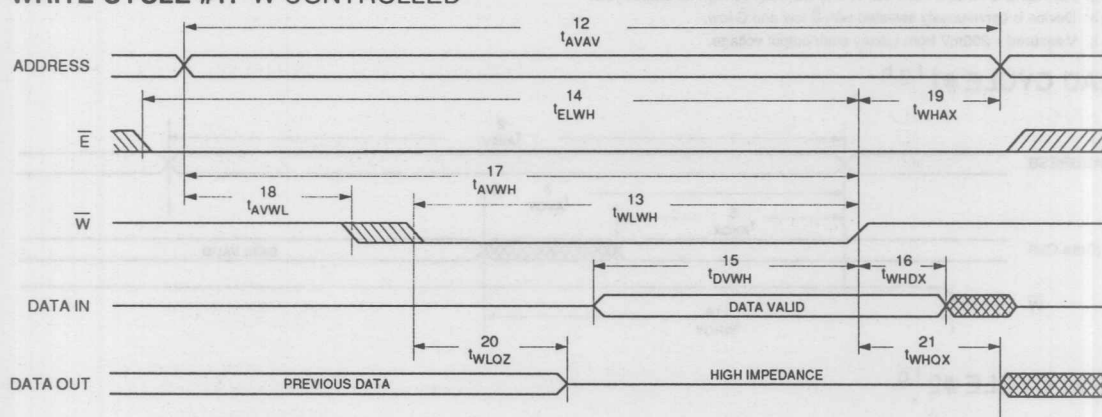
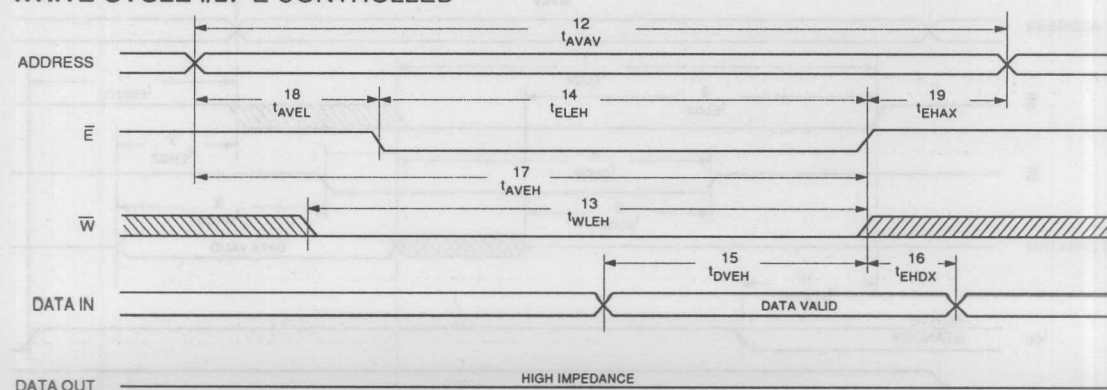
WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	STK20C04-30		STK20C04-35		STK20C04-45		UNITS
	#1	#2	#3		MIN	MAX	MIN	MAX	MIN	MAX	
12	t _{AVAV}	t _{AVAV}	t _{WC}	Write Cycle Time	45		45		45		ns
13	t _{WLWH}	t _{WLEH}	t _{WP}	Write Pulse Width	35		35		35		ns
14	t _{ELWH}	t _{ELEH}	t _{CW}	Chip Enable to End of Write	35		35		35		ns
15	t _{DVWH}	t _{DVEH}	t _{DW}	Data Set-up to End of Write	30		30		30		ns
16	t _{WHDX}	t _{EHDx}	t _{DH}	Data Hold After End of Write	0		0		0		ns
17	t _{AVWH}	t _{AVEH}	t _{AW}	Address Set-up to End of Write	35		35		35		ns
18	t _{AVWL}	t _{AVEL}	t _{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t _{WHAX}	t _{EHAX}	t _{WR}	Address Hold After End of Write	0		0		0		ns
20	t _{WLOZ} ^{i,m}		t _{WZ}	Write Enable to Output Disable		35		35		35	ns
21	t _{WHOX}		t _{OW}	Output Active After End of Write	5		5		5		ns

Note f: $\overline{NE}$ must be high during entire cycle.

Note i: Measured ± 200mV from steady state output voltage.

Note k: $\overline{E}$ or $\overline{W}$ must be high during address transitions.Note m: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.WRITE CYCLE #1: $\overline{W}$ CONTROLLED f,kWRITE CYCLE #2: $\overline{E}$ CONTROLLED f,k

NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\bar{E}$	$\bar{W}$	$\bar{G}$	$\bar{NE}$	MODE	POWER
H	X	X	X	Not Selected	Standby
L	H	L	H	Read RAM	Active
L	L	X	H	Write RAM	Active
L	H	L	L	Nonvolatile <i>RECALL</i> ⁿ	Active
L	L	H	L	Nonvolatile <i>STORE</i>	I_{CC2}
L	L	L	L	No operation	Active
L	H	H	X		

2

STORE CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt.				
22	t_{WLOX}^p	t_{ELOXS}	t_{STORE}	STORE Cycle Time		10	ms
23	t_{WLNH}^q	t_{ELNHS}	t_{WC}	STORE Initiation Cycle Time	25		ns
24	t_{GHNL}			Output Disable Set-up to $\bar{NE}$ Fall	5		ns
25		t_{GHLE}		Output Disable Set-up to $\bar{E}$ Fall	5		ns
26	t_{NLWL}	t_{NLEL}		$\bar{NE}$ Set-up	5		ns
27	t_{ELWL}			Chip Enable Set-up	5		ns
28		t_{WLEL}		Write Enable Set-up	5		ns

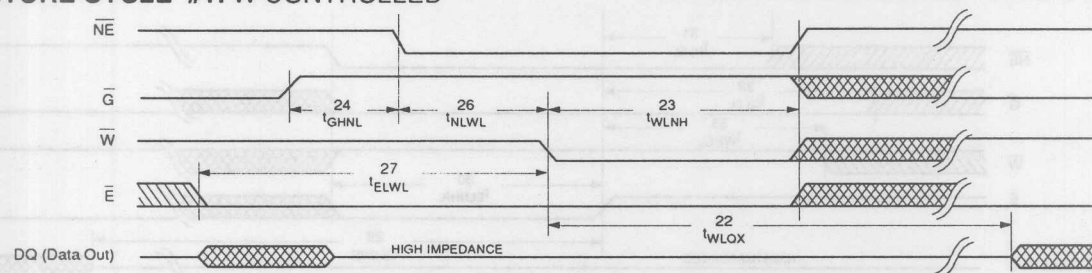
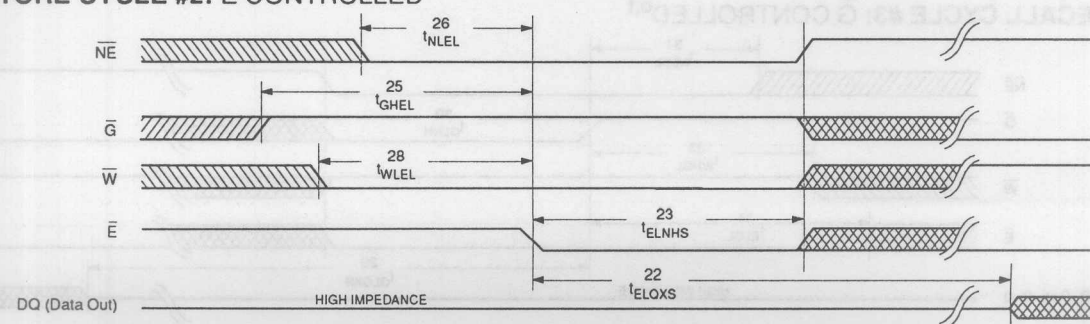
Note n: An automatic *RECALL* also takes place at power up, starting when V_{CC} exceeds 4.0V, and taking t_{RECALL} from the time at which V_{CC} exceeds 4.5V.

V_{CC} must not drop below 4.0V once it has been exceeded for the *RECALL* to function properly.

Note o: If $\bar{E}$ is low for any period of time in which $\bar{W}$ is high while $\bar{G}$ and $\bar{NE}$ are low, then a *RECALL* cycle may be initiated.

Note p: Measured with $\bar{W}$ and $\bar{NE}$ both returned high, and $\bar{G}$ returned low. Note that *STORE* cycles are inhibited/aborted by $V_{CC} < 4.0V$ (*STORE* inhibit).

Note q: Once t_{WC} has been satisfied by $\bar{NE}$, $\bar{G}$, $\bar{W}$ and $\bar{E}$, the *STORE* cycle is completed automatically. Any of $\bar{NE}$, $\bar{G}$, $\bar{W}$ or $\bar{E}$ may be used to terminate the *STORE* initiation cycle.

STORE CYCLE #1: $\bar{W}$ CONTROLLED^oSTORE CYCLE #2: $\bar{E}$ CONTROLLED^o

RECALL CYCLES #1, #2 & #3

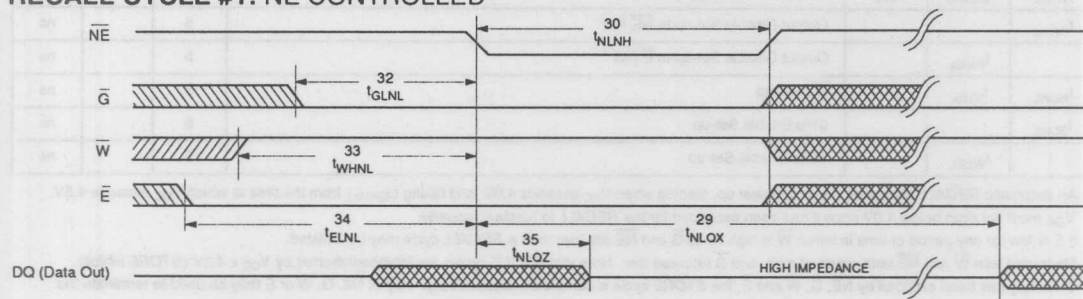
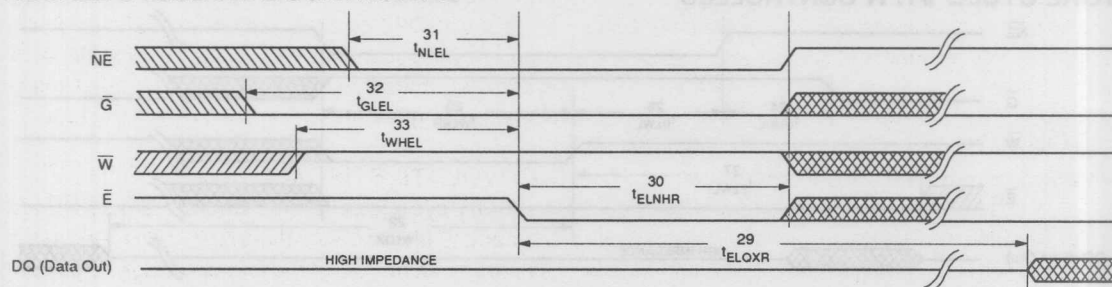
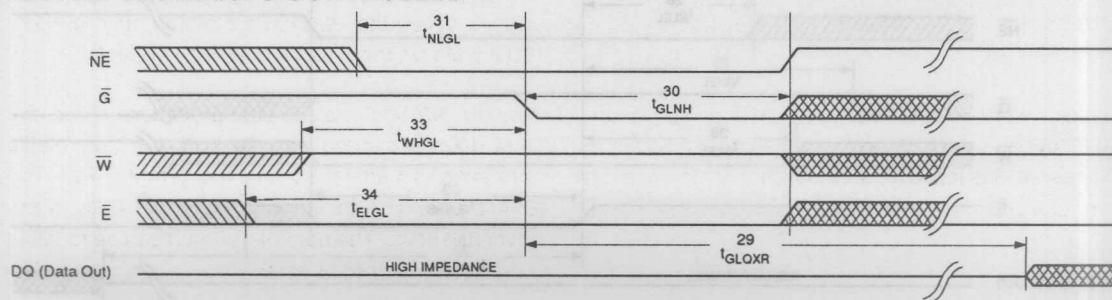
(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt				
29	t _{NLOX} [†]	t _{ELOXR}	t _{GLOXR}	RECALL Cycle Time		20	μs
30	t _{NLNH} ^s	t _{ELNHR}	t _{GLNH}	RECALL Initiation Cycle Time	25		ns
31		t _{NLEL}	t _{NLGL}	$\overline{NE}$ Set-up	5		ns
32	t _{GLNL}	t _{GLEL}		Output Enable Set-up	5		ns
33	t _{WHNL}	t _{WHEL}	t _{WHGL} [†]	Write Enable Set-up	5		ns
34	t _{ELNL}		t _{ELGL}	Chip Enable Set-up	5		ns
35	t _{NLOZ}			$\overline{NE}$ Fall to Outputs Inactive		25	ns

Note r: Measured with $\overline{W}$ and $\overline{NE}$ both high, and $\overline{G}$ and $\overline{E}$ low.

Note s: Once t_{NLNH} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the RECALL cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$ or $\overline{E}$ may be used to terminate the RECALL initiation cycle.

Note t: If $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ is high, then a STORE cycle will be initiated instead of a RECALL.

RECALL CYCLE #1: $\overline{NE}$ CONTROLLED^oRECALL CYCLE #2: $\overline{E}$ CONTROLLED^oRECALL CYCLE #3: $\overline{G}$ CONTROLLED^{o,t}

DEVICE OPERATION

The STK20C04 has two modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pin. When in SRAM mode, the memory operates as a standard fast static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

SRAM READ

The STK20C04 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{NE}$ and $\overline{W}$ are HIGH. The address specified on pins A_{0-8} determines which of the 512 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELOV} or at t_{GLOV} whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{NE}$ is brought LOW.

The STK20C04 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1 μ F connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVVH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLOZ} after $\overline{W}$ goes LOW.

NONVOLATILE STORE

A STORE cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are LOW and $\overline{G}$ is HIGH. While any sequence to achieve this state will initiate a STORE, only $\overline{W}$ initiation (STORE CYCLE #1) and $\overline{E}$ initiation (STORE CYCLE #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a STORE cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a STORE cycle is initiated, further input and output is disabled and the DQ_{0-7} pins are tri-stated until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the STORE.

HARDWARE PROTECT

The STK20C04 offers two levels of protection to suppress inadvertent STORE cycles. If the control signals ($\overline{E}$, $\overline{G}$, $\overline{W}$, and $\overline{NE}$) remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will not be started. The STORE (or RECALL) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the STK20C04 offers hardware protection through V_{CC} Sense. A STORE cycle will not be initiated, and one in progress will discontinue if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC} = 5.0 \pm 10\%$.

NONVOLATILE RECALL

A RECALL cycle is performed when $\overline{E}$, $\overline{G}$, and $\overline{NE}$ are LOW and $\overline{W}$ is HIGH. Like the STORE cycle, RECALL is initiated when the last of the four clock signals goes to the RECALL state. Once initiated, the RECALL cycle will take t_{NLOX} to complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pins will take effect.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the *STORE* cycle, a transition must occur on any control pin to cause a recall, preventing inadvertent multi-triggering. On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.0V once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{NLOX}

after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK20C04 is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system V_{CC} .

ORDERING INFORMATION

2

STK20C04 - W 35 I

Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

30 = 30ns

35 = 35ns

45 = 45ns

Package

W = Plastic 28 pin 600 mil DIP

16 kilobit nvSRAM Products 3



STK10C48

CMOS nvSRAM

High Performance

2K x 8 Nonvolatile Static RAM

FEATURES

- 30, 35 and 45ns Access Times
- 15, 20 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Hardware *STORE* Initiation
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Hardware *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single 5V±10% Operation
- Commercial and Industrial Temperatures
- Available in multiple standard packages

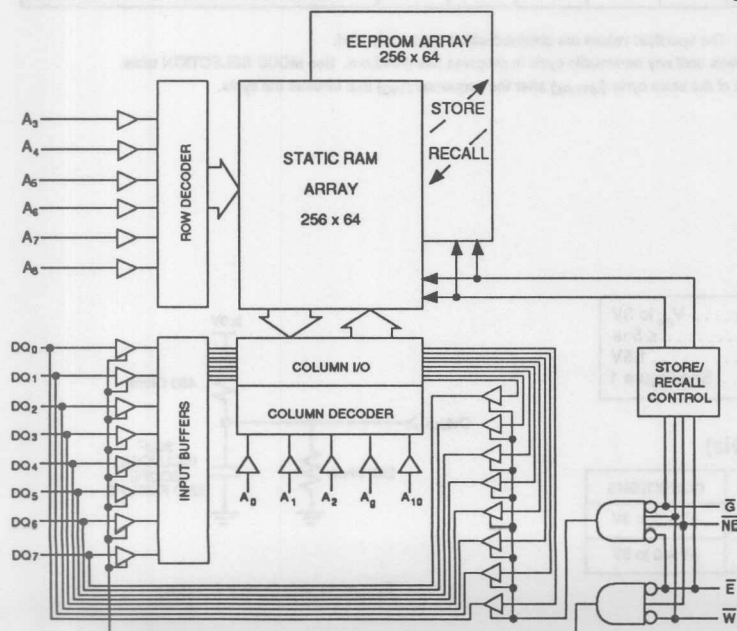
DESCRIPTION

The Simtek STK10C48 is a fast static RAM (30, 35, 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) using the NE pin. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

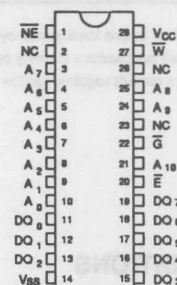
The STK10C48 features the industry standard pinout for nonvolatile RAMs in a 28-pin 300 mil plastic DIP, 28-pin 600 mil plastic DIP, and 28-pin SOIC package.

3

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 350 SOIC
28 - 300 PDIP
28 - 600 PDIP

PIN NAMES

$A_0 - A_{10}$	Address Inputs
$\bar{W}$	Write Enable
$DQ_0 - DQ_7$	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{NE}$	Nonvolatile Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS}	-0.6V to 7.0V
Voltage on DQ_0 and $\bar{G}$	-0.5V to ($V_{CC}+0.5V$)
Temperature under bias	-55°C to 125°C
Storage temperature	-65°C to 150°C
Power dissipation	1W
DC output current	15mA

(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		85		90	mA	$t_{AVAV} = 30ns$
			80		85	mA	$t_{AVAV} = 35ns$
			75		80	mA	$t_{AVAV} = 45ns$
I_{CC2}^d	Average V_{CC} Current during STORE cycle		50		50	mA	All inputs at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		27		30	mA	$t_{AVAV} = 30ns$
			23		27	mA	$t_{AVAV} = 35ns$
			20		23	mA	$t_{AVAV} = 45ns$
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\bar{E} \geq V_{IH}$; all others cycling
							$\bar{E} \geq (V_{CC} - 0.2V)$
I_{LK}	Input Leakage Current (Any Input)		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS} \text{ to } V_{CC}$
I_{OLK}	Off State Output Leakage Current		± 5		± 5	μA	$V_{CC} = \max$ $V_{IN} = V_{SS} \text{ to } V_{CC}$
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: I_{CC2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	$\leq 5ns$
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE^e ($T_A = 25^\circ C$, $f = 1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	$\Delta V = 0 \text{ to } 3V$
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0 \text{ to } 3V$

Note e: These parameters are guaranteed but not tested.

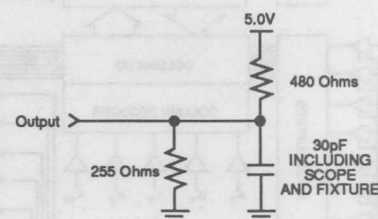


Figure 1: AC Output Loading

READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK10C48-30		STK10C48-35		STK10C48-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t _{ELOV}	t _{ACS}	Chip Enable Access Time		30		35		45	ns
2	t _{AVAV} ^g	t _{RC}	Read Cycle Time	30		35		45		ns
3	t _{AVOV} ^h	t _{AA}	Address Access Time		30		35		45	ns
4	t _{GLOV}	t _{OE}	Output Enable to Data Valid		15		20		25	ns
5	t _{AXOX}	t _{OH}	Output Hold After Address Change	5		5		5		ns
6	t _{ELOX}	t _{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t _{EHQZ} ^l	t _{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t _{GLOX}	t _{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t _{GHOZ} ^l	t _{OHZ}	Output Disable to Output Inactive		15		17		20	ns
10	t _{ELICCH} ^o	t _{PA}	Chip Enable to Power Active	0		0		0		ns
11	t _{EHICCL} ^{c,e}	t _{PS}	Chip Disable to Power Standby		30		35		45	ns
11A	t _{WHQV}	t _{WR}	Write Recovery Time		35		45		55	ns

Note c: Bringing $\bar{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

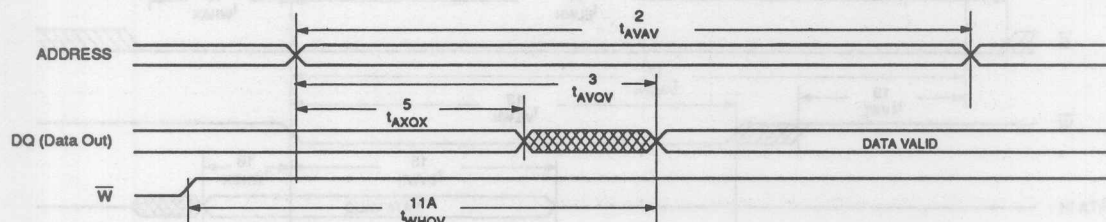
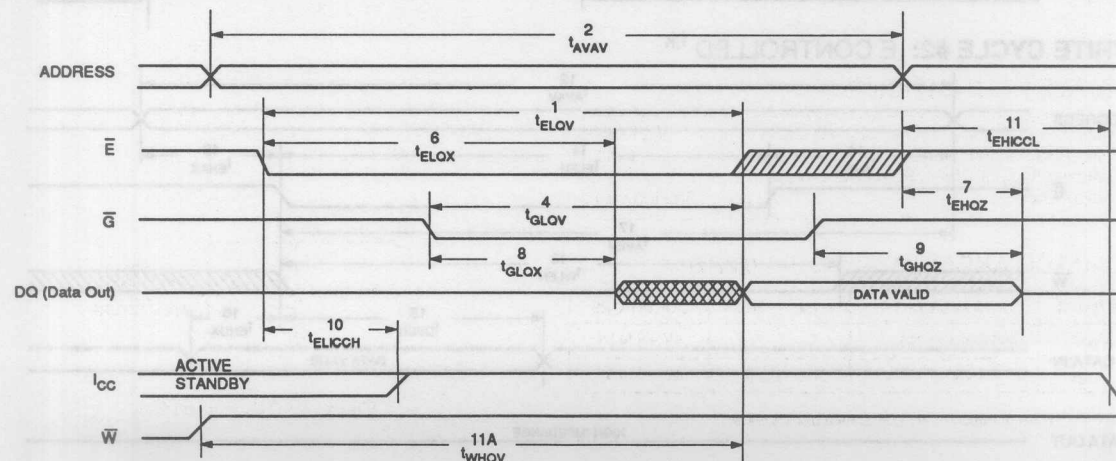
Note e: Parameter guaranteed but not tested.

Note f: $\bar{NE}$ must be high during entire cycle.

Note g: For READ CYCLE #1 and #2, $\bar{W}$ and $\bar{NE}$ must be high for entire cycle.

Note h: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

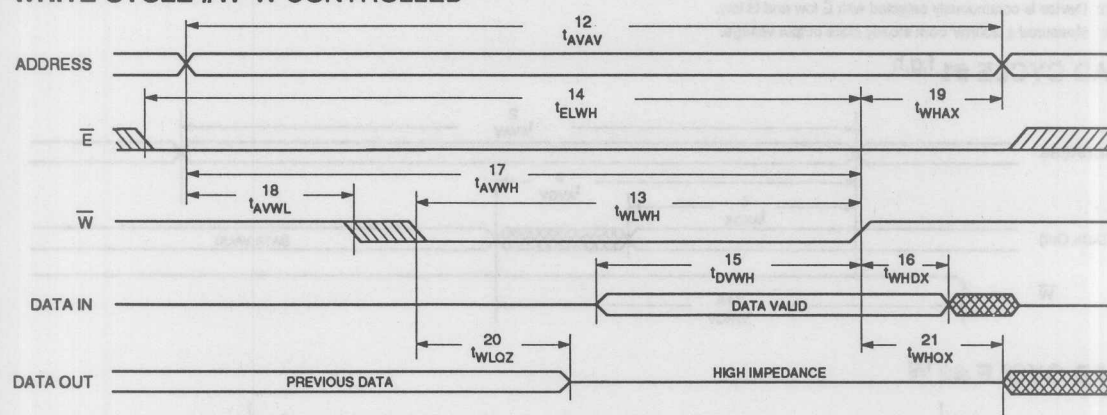
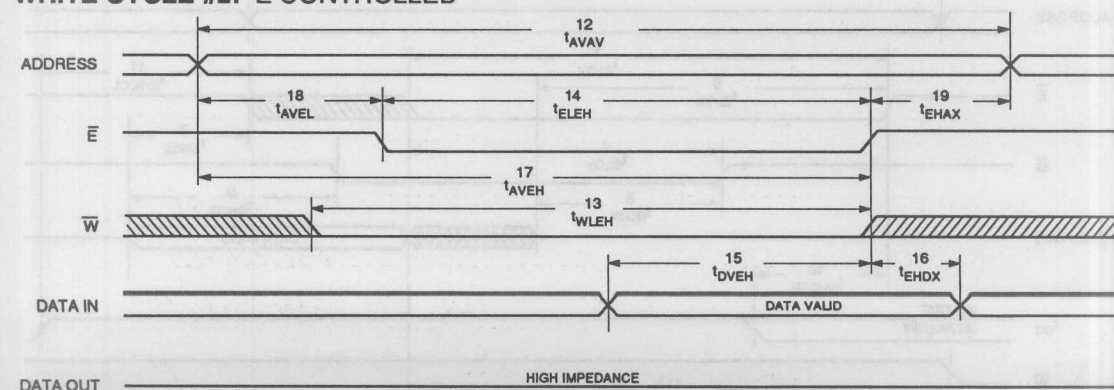
Note i: Measured ± 200mV from steady state output voltage.

READ CYCLE #1^{f,g,h}READ CYCLE #2^{f,g}

WRITE CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	STK10C48-30		STK10C48-35		STK10C48-45		UNITS
	#1	#2	Alt		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	45		45		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	35		35		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	35		35		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	30		30		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	35		35		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	$t_{WLOZ}^{1,m}$		t_{WZ}	Write Enable to Output Disable		35		35		35	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note f: $\overline{NE}$ must be high during entire cycle.Note i: Measured $\pm 200mV$ from steady state output voltage.Note k: $\overline{E}$ or $\overline{W}$ must be high during address transitions.Note m: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.WRITE CYCLE #1: $\overline{W}$ CONTROLLED f,kWRITE CYCLE #2: $\overline{E}$ CONTROLLED f,k

NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$	MODE	POWER
H	X	X	X	Not Selected	Standby
L	H	L	H	Read RAM	Active
L	L	X	H	Write RAM	Active
L	H	L	L	Nonvolatile <i>RECALL</i> ⁿ	Active
L	L	H	L	Nonvolatile <i>STORE</i>	I_{CC2}
L	L	L	L	No operation	Active
L	H	H	X		

STORE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt				
22	t_{WLOX}^p	t_{ELOXS}	t_{STORE}	STORE Cycle Time		10	ms
23	t_{WLNH}^q	t_{ELNHS}	t_{WC}	STORE Initiation Cycle Time	25		ns
24	t_{GHNL}			Output Disable Set-up to $\overline{NE}$ Fall	5		ns
25		t_{GHLE}		Output Disable Set-up to $\overline{E}$ Fall	5		ns
26	t_{NLWL}	t_{NLEL}		$\overline{NE}$ Set-up	5		ns
27	t_{ELWL}			Chip Enable Set-up	5		ns
28		t_{WLEL}		Write Enable Set-up	5		ns

Note n: An automatic *RECALL* also takes place at power up, starting when V_{CC} exceeds 4.0V, and taking t_{RECALL} from the time at which V_{CC} exceeds 4.5V.

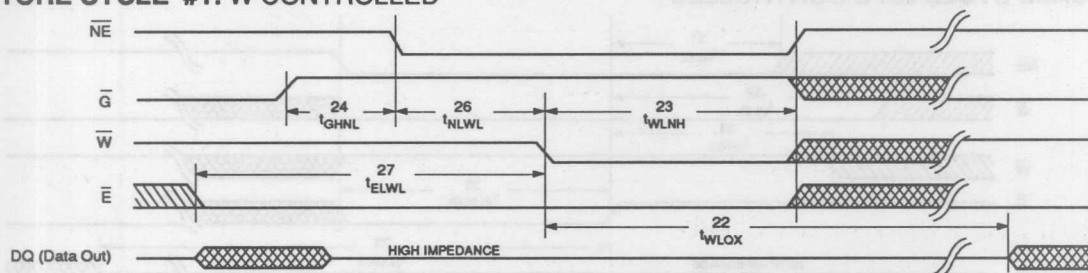
V_{CC} must not drop below 4.0V once it has exceeded it for the *RECALL* to function properly.

Note o: If $\overline{E}$ is low for any period of time in which $\overline{W}$ is high while $\overline{G}$ and $\overline{NE}$ are low, then a *RECALL* cycle may be initiated.

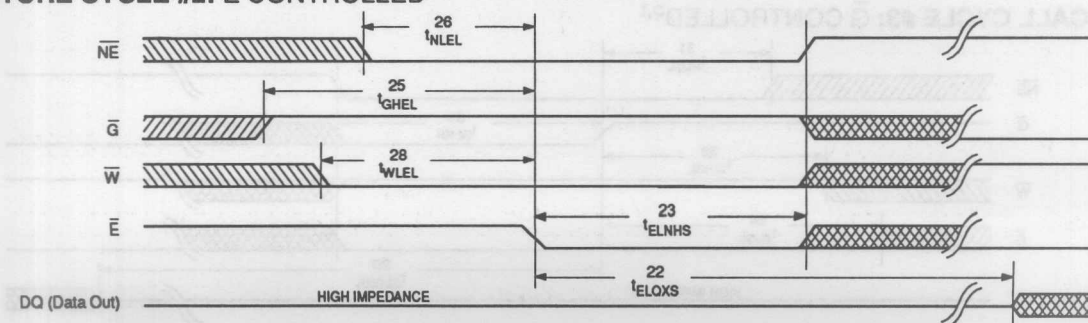
Note p: Measured with $\overline{W}$ and $\overline{NE}$ both returned high, and $\overline{G}$ returned low. Note that *STORE* cycles are inhibited/aborted by V_{CC} < 4.0V (*STORE* inhibit).

Note q: Once t_{WC} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the *STORE* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$, $\overline{W}$ or $\overline{E}$ may be used to terminate the *STORE* initiation cycle.

STORE CYCLE #1: $\overline{W}$ CONTROLLED^o



STORE CYCLE #2: $\overline{E}$ CONTROLLED^o



RECALL CYCLES #1, #2 & #3

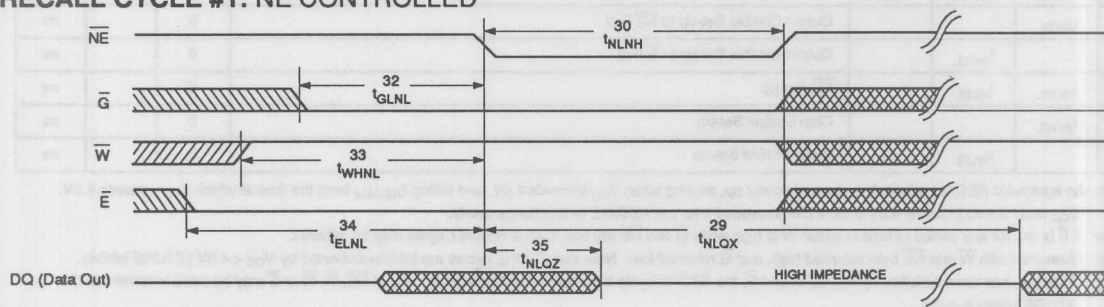
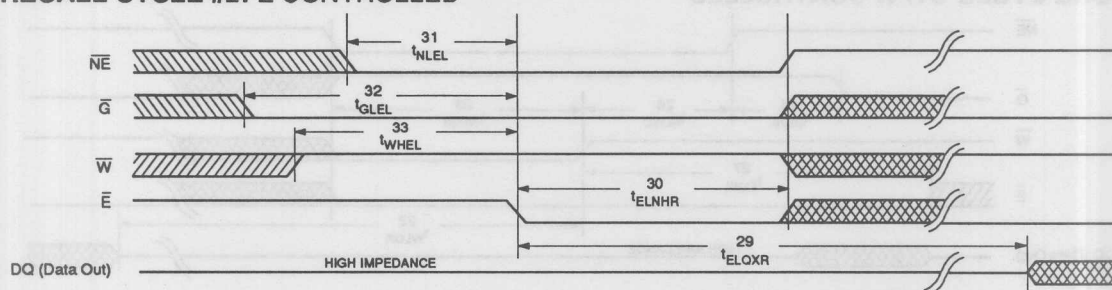
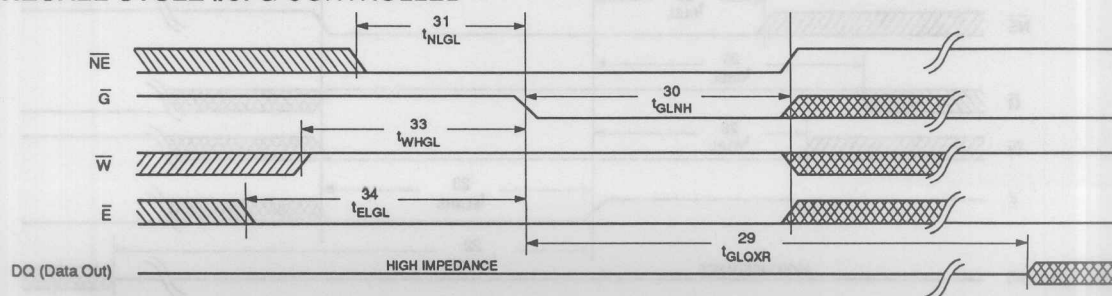
(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	#3				
29	t _{NLOX} [†]	t _{ELOXR}	t _{GLOXR}	RECALL Cycle Time		20	μs
30	t _{NLNH} ^o	t _{ELNHR}	t _{GLNH}	RECALL Initiation Cycle Time	25		ns
31		t _{NLEL}	t _{NLGL}	$\overline{NE}$ Set-up	5		ns
32	t _{GLNL}	t _{GLEL}		Output Enable Set-up	5		ns
33	t _{WHNL}	t _{WHEL}	t _{WHGL} [†]	Write Enable Set-up	5		ns
34	t _{ELNL}		t _{ELGL}	Chip Enable Set-up	5		ns
35	t _{NLOZ}			$\overline{NE}$ Fall to Outputs Inactive		25	ns

Note r: Measured with $\overline{W}$ and $\overline{NE}$ both high, and $\overline{G}$ and $\overline{E}$ low.

Note s: Once t_{NLNH} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the RECALL cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$ or $\overline{E}$ may be used to terminate the RECALL initiation cycle.

Note t: If $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ is high, then a STORE cycle will be Initiated instead of a RECALL.

RECALL CYCLE #1: $\overline{NE}$ CONTROLLED^oRECALL CYCLE #2: $\overline{E}$ CONTROLLED^oRECALL CYCLE #3: $\overline{G}$ CONTROLLED^{o,t}

DEVICE OPERATION

The STK10C48 has two modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pin. When in SRAM mode, the memory operates as a standard fast static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

SRAM READ

The STK10C48 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{NE}$ and $\overline{W}$ are HIGH. The address specified on pins A_{0-10} determines which of the 2048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{NE}$ is brought LOW.

The STK10C48 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1 μF connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes LOW.

NONVOLATILE STORE

A STORE cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are LOW and $\overline{G}$ is HIGH. While any sequence to achieve this state will initiate a STORE, only $\overline{W}$ initiation (STORE CYCLE #1) and $\overline{E}$ initiation (STORE CYCLE #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a STORE cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a STORE cycle is initiated, further input and output is disabled and the DQ_{0-7} pins are tri-stated until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the STORE.

HARDWARE PROTECT

The STK10C48 offers two levels of protection to suppress inadvertent STORE cycles. If the control signals ($\overline{E}$, $\overline{G}$, $\overline{W}$, and $\overline{NE}$) remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will *not* be started. The STORE (or RECALL) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the STK10C48 offers hardware protection through V_{CC} Sense. A STORE cycle will not be initiated, and one in progress will discontinue if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC} = 5.0V \pm 10\%$.

NONVOLATILE RECALL

A RECALL cycle is performed when $\overline{E}$, $\overline{G}$, and $\overline{NE}$ are LOW and $\overline{W}$ is HIGH. Like the STORE cycle, RECALL is initiated when the last of the four clock signals goes to the RECALL state. Once initiated, the RECALL cycle will take t_{NLQX} to complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pins will take effect.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The

nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the *STORE* cycle, a transition must occur on any control pin to cause a recall, preventing inadvertent multi-triggering. On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.0V once it has risen above it in order for the

RECALL to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{NLOX} after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK10C68 is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system V_{CC} .

ORDERING INFORMATION

STK10C48 - P 30 I

Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

30 = 30ns

35 = 35ns

45 = 45ns

Package

P = Plastic 28 pin 300 mil DIP

W = Plastic 28 pin 600 mil DIP

S = Plastic 28 pin SOIC

3

ORDERING INFORMATION

STK10C48 - P 30 1

Temperature Range

Pin 1 - Commercial (0 to 70 degrees C)
Pin 2 - Industrial (-40 to 85 degrees C)

Access Time

30 - 30ns
32 - 32ns
48 - 48ns

Package

P - Plastic 28 pin 300 mil DIP
W - Plastic 28 pin 400 mil DIP
S - Plastic 28 pin SOIC



STK11C48

CMOS nvSRAM

High Performance

2K x 8 Nonvolatile Static RAM

FEATURES

- 30, 35 and 45ns Access Times
- 15, 20 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Software *STORE* Initiation
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Software *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single 5V $\pm$ 10% Operation
- Commercial and Industrial Temperatures
- Available in multiple standard packages

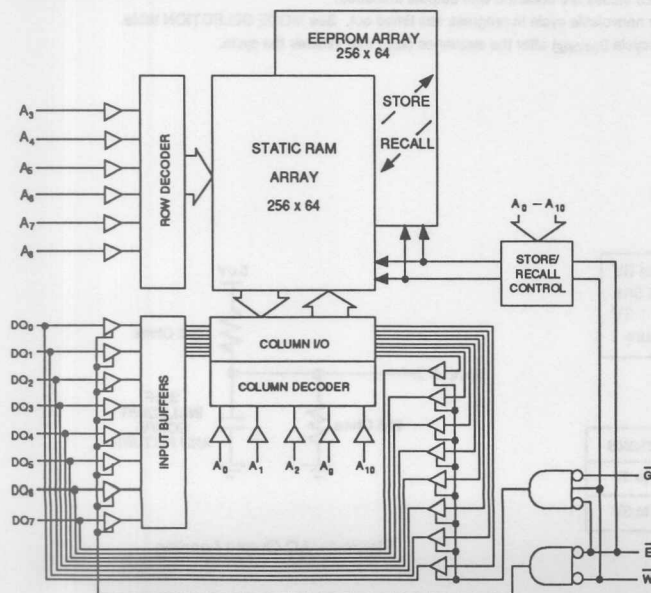
DESCRIPTION

The Simtek STK11C48 is a fast static RAM (30, 35, 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) are initiated through software sequences. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

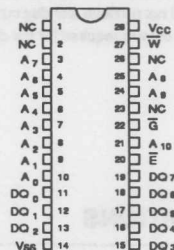
The STK11C48 is pin compatible with industry standard SRAMs and is available in a 28-pin 300 mil plastic DIP, 28-pin 600 mil plastic DIP package and 28 pin SOIC packages.

3

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 350 SOIC
28 - 300 PDIP
28 - 600 PDIP

PIN NAMES

A ₀ - A ₁₀	Address Inputs
W	Write Enable
DQ ₀ - DQ ₇	Data In/Out
E	Chip Enable
G	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS}-0.6V to 7.0V
Voltage on DQ_0 -7 and $\bar{G}$-0.5V to ($V_{CC}+0.5V$)
Temperature under bias.....-55°C to 125°C
Storage temperature.....-65°C to 150°C
Power dissipation.....1W
DC output current.....15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		85		90	mA	$t_{AVAV} = 30ns$
			80		85	mA	$t_{AVAV} = 35ns$
			75		80	mA	$t_{AVAV} = 45ns$
I_{CC2}^d	Average V_{CC} Current during STORE cycle		50		50	mA	All inputs at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		27		30	mA	$t_{AVAV} = 30ns$
			23		27	mA	$t_{AVAV} = 35ns$
			20		23	mA	$t_{AVAV} = 45ns$
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\bar{E} \geq V_{IH}$; all others cycling
							$E \geq (V_{CC} - 0.2V)$
							all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{LK}	Input Leakage Current (Any Input)		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5		± 5	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note d: I_{CC2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels..... V_{SS} to 3V
Input Rise and Fall Times..... $\leq 5ns$
Input and Output Timing Reference Levels..... 1.5V
Output Load..... See Figure 1

CAPACITANCE^e ($T_A=25^\circ C, f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

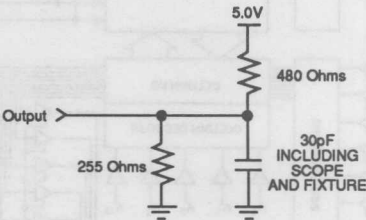


Figure 1: AC Output Loading

READ CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK11C48-30		STK11C48-35		STK11C48-45		UNITS
	#1, #2	Alt		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELOV}	t_{ACS}	Chip Enable Access Time		30		35		45	ns
2	t_{AVAV}^g	t_{RC}	Read Cycle Time	30		35		45		ns
3	t_{AVOV}^h	t_{AA}	Address Access Time		30		35		45	ns
4	t_{GLOV}	t_{OE}	Output Enable to Data Valid		15		20		25	ns
5	t_{AXOX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELOX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHOZ}	t_{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t_{GLOX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHOZ}	t_{OHZ}	Output Disable to Output Inactive		15		17		20	ns
10	t_{ELICCH}^e	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{c,e}$	t_{PS}	Chip Disable to Power Standby		30		35		45	ns
11A	t_{WHOV}	t_{WR}	Write Recovery Time		35		45		55	ns

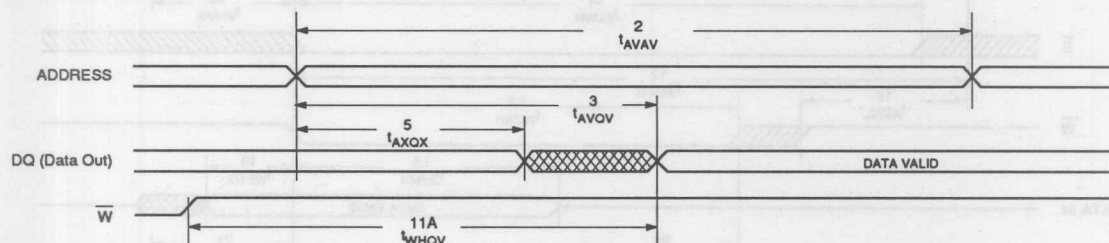
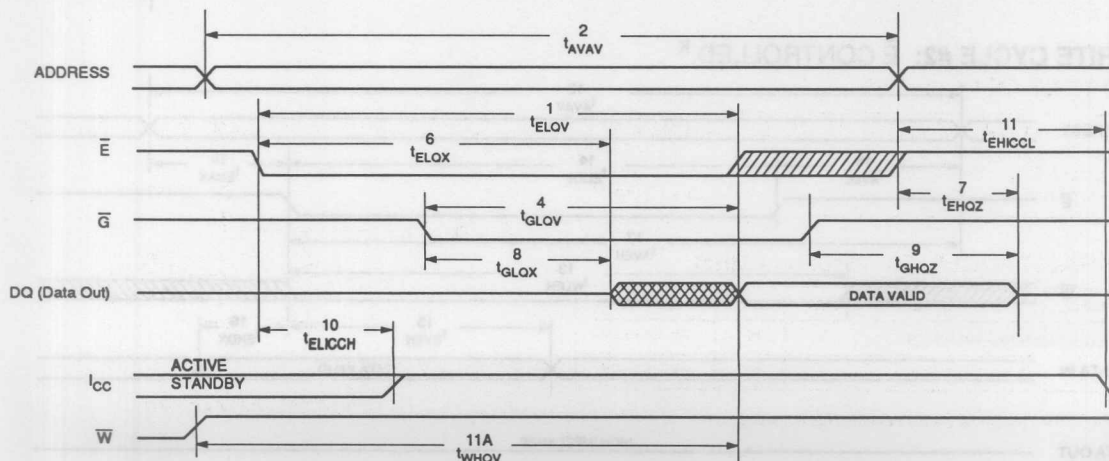
Note c: Bringing $\bar{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note e: Parameter guaranteed but not tested.

Note g: For READ CYCLE #1 and #2, $\bar{W}$ must be high for entire cycle.

Note h: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note I: Measured $\pm 200mV$ from steady state output voltage.

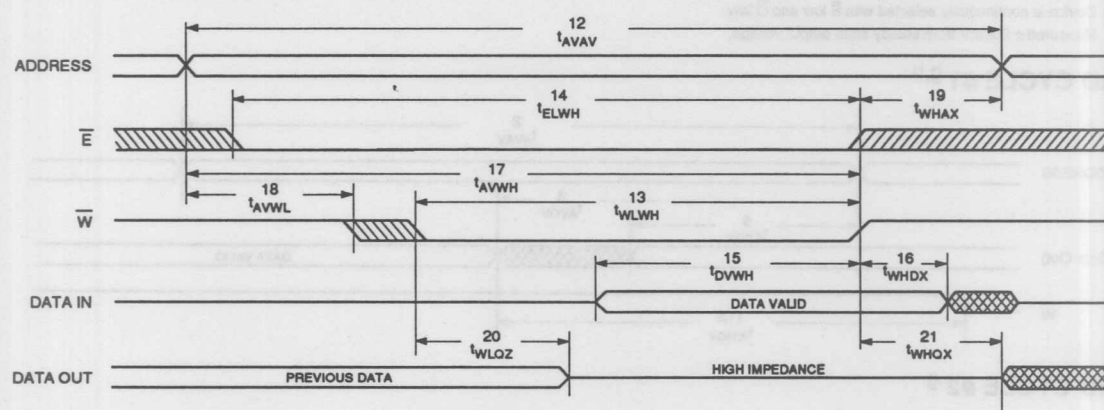
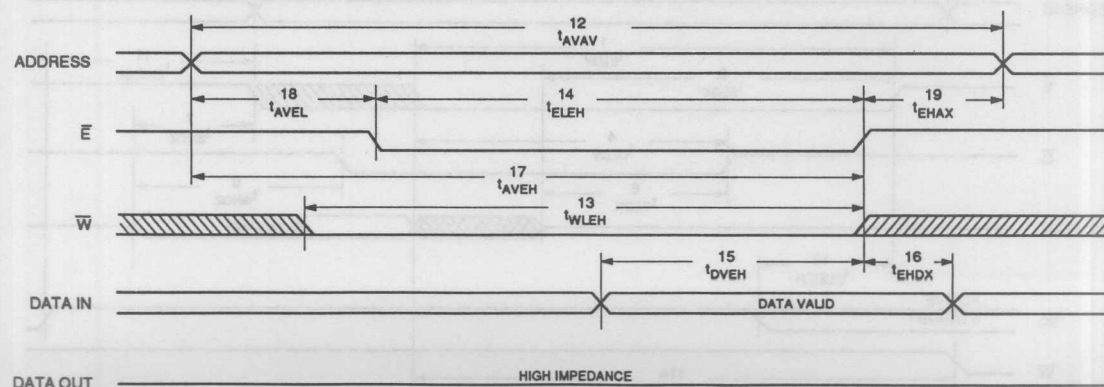
READ CYCLE #1 ^{g,h}READ CYCLE #2 ^g

WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	STK11C48-30		STK11C48-35		STK11C48-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t _{AVAV}	t _{AVAV}	t _{WC}	Write Cycle Time	45		45		45		ns
13	t _{WLWH}	t _{WLEH}	t _{WP}	Write Pulse Width	35		35		35		ns
14	t _{ELWH}	t _{ELEH}	t _{CW}	Chip Enable to End of Write	35		35		35		ns
15	t _{DVWH}	t _{DVEH}	t _{DW}	Data Set-up to End of Write	30		30		30		ns
16	t _{WHDX}	t _{EHDH}	t _{DH}	Data Hold After End of Write	0		0		0		ns
17	t _{AVWH}	t _{AVEH}	t _{AW}	Address Set-up to End of Write	35		35		35		ns
18	t _{AVWL}	t _{AVEL}	t _{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t _{WHAX}	t _{EHAX}	t _{WR}	Address Hold After End of Write	0		0		0		ns
20	t _{WLOZ} ^{1,m}		t _{WZ}	Write Enable to Output Disable		35		35		35	ns
21	t _{WHQX}		t _{OW}	Output Active After End of Write	5		5		5		ns

Note i: Measured ±200mV from steady state output voltage.

Note k: $\bar{E}$ or $\bar{W}$ must be high during address transitions.Note m: If $\bar{W}$ is low when $\bar{E}$ goes low, the outputs remain in the high impedance state.WRITE CYCLE #1: $\bar{W}$ CONTROLLED^kWRITE CYCLE #2: $\bar{E}$ CONTROLLED^k

NONVOLATILE MEMORY OPERATION

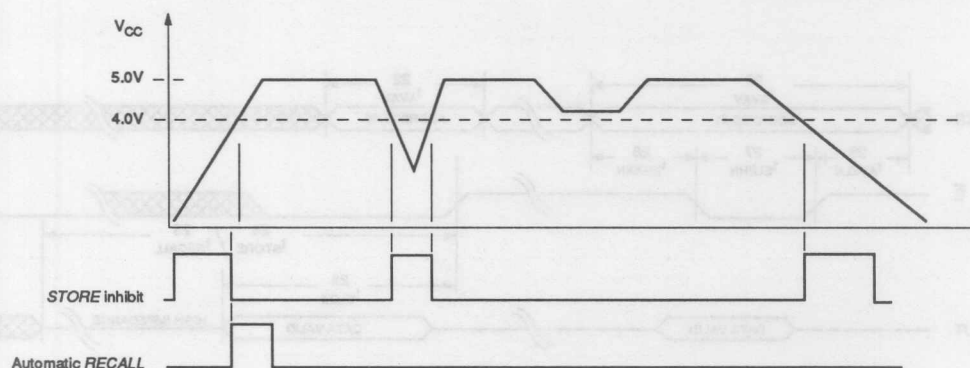
MODE SELECTION

$\bar{E}$	$\bar{W}$	$A_{10} - A_0(\text{hex})$	MODE	I/O	POWER	NOTES
H	X	X	Not Selected	Output High Z	Standby	
L	H	X	Read SRAM	Output Data	Active	o
L	L	X	Write SRAM	Input Data	Active	
L	H	000	Read SRAM	Output Data	Active	n,o
		555	Read SRAM	Output Data		n,o
		2AA	Read SRAM	Output Data		n,o
		7FF	Read SRAM	Output Data		n,o
		0F0	Read SRAM	Output Data		n,o
		70F	Nonvolatile <i>STORE</i>	Output High Z		n
L	H	000	Read SRAM	Output Data	Active	n,o
		555	Read SRAM	Output Data		n,o
		2AA	Read SRAM	Output Data		n,o
		7FF	Read SRAM	Output Data		n,o
		0F0	Read SRAM	Output Data		n,o
		70E	Nonvolatile <i>RECALL</i>	Output High Z		n

Note n: The six consecutive addresses must be in order listed - (000, 555, 2AA, 7FF, 0F0, 70F) for a *STORE* cycle or (000, 555, 2AA, 7FF, 0F0, 70E) for a *RECALL* cycle. $\bar{W}$ must be high during all six consecutive cycles. See *STORE* cycle and *RECALL* cycle tables and diagrams for further details.

Note o: I/O state assumes that $\bar{G}$ is low. Initiation and operation of nonvolatile cycles does not depend on the state of $\bar{G}$.

STORE CYCLE INHIBIT and AUTOMATIC POWER-UP RECALL



STORE/RECALL CYCLE

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK11C48-30		STK11C48-35		STK11C48-45		UNITS
	#1	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
22	t _{AVAV}	t _{RC}	STORE/RECALL Initiation Cycle Time	30		35		45		ns
23	t _{ELOZ} ^p		Chip Enable to Output Inactive		75		75		75	ns
24	t _{ELOXS}	t _{STORE} ^q	STORE Cycle Time		10		10		10	ms
25	t _{ELOXR}	t _{RECALL} ^r	RECALL Cycle Time		20		20		20	μs
26	t _{AVELN} ^s	t _{AE}	Address Set-up to Chip Enable	0		0		0		ns
27	t _{ELEHN} ^{s,t}	t _{EP}	Chip Enable Pulse Width	20		25		35		ns
28	t _{EHAXN} ^s	t _{EA}	Chip Disable to Address Change	0		0		0		ns

Note p: Once the software *STORE* or *RECALL* cycle is initiated, it completes automatically, ignoring all inputs.

Note q: Note that *STORE* cycles (but not *RECALL*s) are aborted by V_{CC} < 4.0V (*STORE* inhibit).

Note r: A *RECALL* cycle is initiated automatically at power up when V_{CC} exceeds 4.0V. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

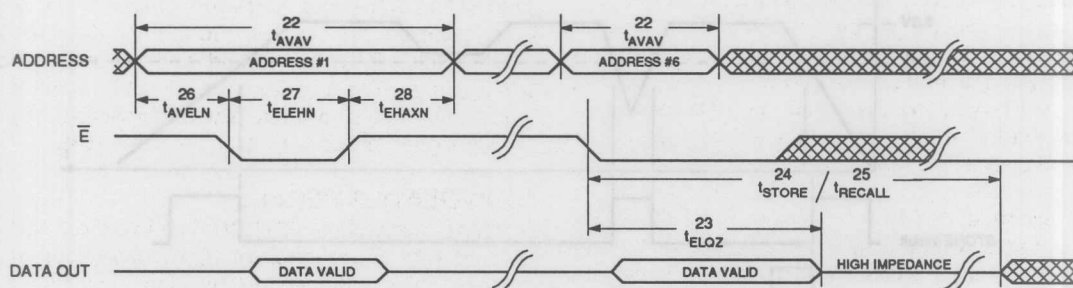
Note s: Noise on the $\bar{E}$ pin may trigger multiple read cycles from the same address and abort the address sequence.

Note t: If the Chip Enable Pulse Width is less than t_{ELOV} (see *READ CYCLE #2*) but greater than or equal to t_{ELEHN}, then the data may not be valid at the end of the low pulse, however the *STORE* or *RECALL* will still be initiated.

Note u: $\bar{W}$ must be HIGH when $\bar{E}$ is Low during the address sequence in order to initiate a nonvolatile cycle. $\bar{G}$ may be either HIGH or LOW throughout.

Addresses #1 through #6 are found in the *MODE SELECTION* table. Address #6 determines whether the STK11C48 performs a *STORE* or *RECALL*.

Note v: $\bar{E}$ must be used to clock in the address sequence for the Software *STORE* and *RECALL* cycles.

STORE/RECALL CYCLE ^{u,v}

DEVICE OPERATION

The STK11C48 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile operation, data is transferred from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

SRAM READ

The STK11C48 performs a READ cycle whenever $\bar{E}$ and $\bar{G}$ are LOW while $\bar{W}$ is HIGH. The address specified on pins A_{0-10} determines which of the 2048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\bar{E}$ or $\bar{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\bar{E}$ or $\bar{G}$ is brought HIGH or $\bar{W}$ is brought LOW.

The STK11C48 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately $0.1\mu F$ connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\bar{E}$ and $\bar{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\bar{E}$ or $\bar{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{PVWH} before the end of a $\bar{W}$ controlled WRITE or t_{DVEH} before the end of an $\bar{E}$ controlled WRITE.

It is recommended that $\bar{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\bar{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLOZ} after $\bar{W}$ goes LOW.

NONVOLATILE STORE

The STK11C48 *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the STK11C48 implements nonvolatile operation while remaining pin-for-pin compatible with standard 2Kx8 SRAMs. During

the *STORE* cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for *STORE* initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To enable the *STORE* cycle the following READ sequence must be performed:

- | | | |
|-----------------|-----------|-----------------------------|
| 1. Read address | 000 (hex) | Valid READ |
| 2. Read address | 555 (hex) | Valid READ |
| 3. Read address | 2AA (hex) | Valid READ |
| 4. Read address | 7FF (hex) | Valid READ |
| 5. Read address | 0F0 (hex) | Valid READ |
| 6. Read address | 70F (hex) | Initiate <i>STORE</i> Cycle |

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\bar{G}$ be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

HARDWARE PROTECT

The STK11C48 offers hardware protection against inadvertent *STORE* cycles through V_{CC} Sense. A *STORE* cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC} = 5.0 \pm 10\%$.

NONVOLATILE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operation must be performed:

- | | | |
|-----------------|-----------|------------------------------|
| 1. Read address | 000 (hex) | Valid READ |
| 2. Read address | 555 (hex) | Valid READ |
| 3. Read address | 2AA (hex) | Valid READ |
| 4. Read address | 7FF (hex) | Valid READ |
| 5. Read address | 0F0 (hex) | Valid READ |
| 6. Read address | 70E (hex) | Initiate <i>RECALL</i> Cycle |

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.0V

once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{RECALL} after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK11C48 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\bar{W}$ and system V_{CC} .

3

To enable the STORE cycle the following READ sequence must be performed:

1. Read address 000 (hex)	Valid READ
2. Read address 000 (hex)	Valid READ
3. Read address 000 (hex)	Valid READ
4. Read address 000 (hex)	Valid READ
5. Read address 000 (hex)	Valid READ
6. Read address 000 (hex)	Valid READ
7. Read address 000 (hex)	Valid READ
8. Read address 000 (hex)	Valid READ
9. Read address 000 (hex)	Valid READ
10. Read address 000 (hex)	Valid READ
11. Read address 000 (hex)	Valid READ
12. Read address 000 (hex)	Valid READ
13. Read address 000 (hex)	Valid READ
14. Read address 000 (hex)	Valid READ
15. Read address 000 (hex)	Valid READ
16. Read address 000 (hex)	Valid READ
17. Read address 000 (hex)	Valid READ
18. Read address 000 (hex)	Valid READ
19. Read address 000 (hex)	Valid READ
20. Read address 000 (hex)	Valid READ
21. Read address 000 (hex)	Valid READ
22. Read address 000 (hex)	Valid READ
23. Read address 000 (hex)	Valid READ
24. Read address 000 (hex)	Valid READ
25. Read address 000 (hex)	Valid READ
26. Read address 000 (hex)	Valid READ
27. Read address 000 (hex)	Valid READ
28. Read address 000 (hex)	Valid READ
29. Read address 000 (hex)	Valid READ
30. Read address 000 (hex)	Valid READ
31. Read address 000 (hex)	Valid READ
32. Read address 000 (hex)	Valid READ
33. Read address 000 (hex)	Valid READ
34. Read address 000 (hex)	Valid READ
35. Read address 000 (hex)	Valid READ
36. Read address 000 (hex)	Valid READ
37. Read address 000 (hex)	Valid READ
38. Read address 000 (hex)	Valid READ
39. Read address 000 (hex)	Valid READ
40. Read address 000 (hex)	Valid READ
41. Read address 000 (hex)	Valid READ
42. Read address 000 (hex)	Valid READ
43. Read address 000 (hex)	Valid READ
44. Read address 000 (hex)	Valid READ
45. Read address 000 (hex)	Valid READ
46. Read address 000 (hex)	Valid READ
47. Read address 000 (hex)	Valid READ
48. Read address 000 (hex)	Valid READ
49. Read address 000 (hex)	Valid READ
50. Read address 000 (hex)	Valid READ
51. Read address 000 (hex)	Valid READ
52. Read address 000 (hex)	Valid READ
53. Read address 000 (hex)	Valid READ
54. Read address 000 (hex)	Valid READ
55. Read address 000 (hex)	Valid READ
56. Read address 000 (hex)	Valid READ
57. Read address 000 (hex)	Valid READ
58. Read address 000 (hex)	Valid READ
59. Read address 000 (hex)	Valid READ
60. Read address 000 (hex)	Valid READ
61. Read address 000 (hex)	Valid READ
62. Read address 000 (hex)	Valid READ
63. Read address 000 (hex)	Valid READ
64. Read address 000 (hex)	Valid READ
65. Read address 000 (hex)	Valid READ
66. Read address 000 (hex)	Valid READ
67. Read address 000 (hex)	Valid READ
68. Read address 000 (hex)	Valid READ
69. Read address 000 (hex)	Valid READ
70. Read address 000 (hex)	Valid READ
71. Read address 000 (hex)	Valid READ
72. Read address 000 (hex)	Valid READ
73. Read address 000 (hex)	Valid READ
74. Read address 000 (hex)	Valid READ
75. Read address 000 (hex)	Valid READ
76. Read address 000 (hex)	Valid READ
77. Read address 000 (hex)	Valid READ
78. Read address 000 (hex)	Valid READ
79. Read address 000 (hex)	Valid READ
80. Read address 000 (hex)	Valid READ
81. Read address 000 (hex)	Valid READ
82. Read address 000 (hex)	Valid READ
83. Read address 000 (hex)	Valid READ
84. Read address 000 (hex)	Valid READ
85. Read address 000 (hex)	Valid READ
86. Read address 000 (hex)	Valid READ
87. Read address 000 (hex)	Valid READ
88. Read address 000 (hex)	Valid READ
89. Read address 000 (hex)	Valid READ
90. Read address 000 (hex)	Valid READ
91. Read address 000 (hex)	Valid READ
92. Read address 000 (hex)	Valid READ
93. Read address 000 (hex)	Valid READ
94. Read address 000 (hex)	Valid READ
95. Read address 000 (hex)	Valid READ
96. Read address 000 (hex)	Valid READ
97. Read address 000 (hex)	Valid READ
98. Read address 000 (hex)	Valid READ
99. Read address 000 (hex)	Valid READ
100. Read address 000 (hex)	Valid READ

Once the valid address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although a valid address is not necessary for a STORE cycle to be valid. After the STORE cycle has been initiated, the SRAM will again be available for READ and WRITE operations.

HARDWARE PROTECT

The STK11C48 offers hardware protection against inadvertent STORE cycles through V_{CC} Sense. A STORE cycle will not be initiated, and one in progress will be discontinued, if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The device specifications are guaranteed only for $V_{CC} = 5.0 \pm 10\%$.

NONVOLATILE RECALL

A RECALL cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the STORE initiator. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1. Read address 000 (hex)	Valid READ
2. Read address 000 (hex)	Valid READ
3. Read address 000 (hex)	Valid READ
4. Read address 000 (hex)	Valid READ
5. Read address 000 (hex)	Valid READ
6. Read address 000 (hex)	Valid READ
7. Read address 000 (hex)	Valid READ
8. Read address 000 (hex)	Valid READ
9. Read address 000 (hex)	Valid READ
10. Read address 000 (hex)	Valid READ
11. Read address 000 (hex)	Valid READ
12. Read address 000 (hex)	Valid READ
13. Read address 000 (hex)	Valid READ
14. Read address 000 (hex)	Valid READ
15. Read address 000 (hex)	Valid READ
16. Read address 000 (hex)	Valid READ
17. Read address 000 (hex)	Valid READ
18. Read address 000 (hex)	Valid READ
19. Read address 000 (hex)	Valid READ
20. Read address 000 (hex)	Valid READ
21. Read address 000 (hex)	Valid READ
22. Read address 000 (hex)	Valid READ
23. Read address 000 (hex)	Valid READ
24. Read address 000 (hex)	Valid READ
25. Read address 000 (hex)	Valid READ
26. Read address 000 (hex)	Valid READ
27. Read address 000 (hex)	Valid READ
28. Read address 000 (hex)	Valid READ
29. Read address 000 (hex)	Valid READ
30. Read address 000 (hex)	Valid READ
31. Read address 000 (hex)	Valid READ
32. Read address 000 (hex)	Valid READ
33. Read address 000 (hex)	Valid READ
34. Read address 000 (hex)	Valid READ
35. Read address 000 (hex)	Valid READ
36. Read address 000 (hex)	Valid READ
37. Read address 000 (hex)	Valid READ
38. Read address 000 (hex)	Valid READ
39. Read address 000 (hex)	Valid READ
40. Read address 000 (hex)	Valid READ
41. Read address 000 (hex)	Valid READ
42. Read address 000 (hex)	Valid READ
43. Read address 000 (hex)	Valid READ
44. Read address 000 (hex)	Valid READ
45. Read address 000 (hex)	Valid READ
46. Read address 000 (hex)	Valid READ
47. Read address 000 (hex)	Valid READ
48. Read address 000 (hex)	Valid READ
49. Read address 000 (hex)	Valid READ
50. Read address 000 (hex)	Valid READ
51. Read address 000 (hex)	Valid READ
52. Read address 000 (hex)	Valid READ
53. Read address 000 (hex)	Valid READ
54. Read address 000 (hex)	Valid READ
55. Read address 000 (hex)	Valid READ
56. Read address 000 (hex)	Valid READ
57. Read address 000 (hex)	Valid READ
58. Read address 000 (hex)	Valid READ
59. Read address 000 (hex)	Valid READ
60. Read address 000 (hex)	Valid READ
61. Read address 000 (hex)	Valid READ
62. Read address 000 (hex)	Valid READ
63. Read address 000 (hex)	Valid READ
64. Read address 000 (hex)	Valid READ
65. Read address 000 (hex)	Valid READ
66. Read address 000 (hex)	Valid READ
67. Read address 000 (hex)	Valid READ
68. Read address 000 (hex)	Valid READ
69. Read address 000 (hex)	Valid READ
70. Read address 000 (hex)	Valid READ
71. Read address 000 (hex)	Valid READ
72. Read address 000 (hex)	Valid READ
73. Read address 000 (hex)	Valid READ
74. Read address 000 (hex)	Valid READ
75. Read address 000 (hex)	Valid READ
76. Read address 000 (hex)	Valid READ
77. Read address 000 (hex)	Valid READ
78. Read address 000 (hex)	Valid READ
79. Read address 000 (hex)	Valid READ
80. Read address 000 (hex)	Valid READ
81. Read address 000 (hex)	Valid READ
82. Read address 000 (hex)	Valid READ
83. Read address 000 (hex)	Valid READ
84. Read address 000 (hex)	Valid READ
85. Read address 000 (hex)	Valid READ
86. Read address 000 (hex)	Valid READ
87. Read address 000 (hex)	Valid READ
88. Read address 000 (hex)	Valid READ
89. Read address 000 (hex)	Valid READ
90. Read address 000 (hex)	Valid READ
91. Read address 000 (hex)	Valid READ
92. Read address 000 (hex)	Valid READ
93. Read address 000 (hex)	Valid READ
94. Read address 000 (hex)	Valid READ
95. Read address 000 (hex)	Valid READ
96. Read address 000 (hex)	Valid READ
97. Read address 000 (hex)	Valid READ
98. Read address 000 (hex)	Valid READ
99. Read address 000 (hex)	Valid READ
100. Read address 000 (hex)	Valid READ

The STK11C48 is a high speed memory and therefore must have a high frequency bypass capacitor at its power supply. A 10K Ohm resistor should be connected between $\bar{W}$ and V_{CC} and V_{CC} should be connected to ground. The device is not recommended for use in high speed CMOS logic applications. As with all high speed CMOS logic, signals will help to reduce power ground and signals will help to reduce noise problems.

SRAM WRITE

A valid cycle is performed when $\bar{E}$ and $\bar{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\bar{E}$ or $\bar{W}$ goes HIGH at the end of the cycle. The data on pins D_0 through D_7 will be written into the memory if a valid cycle is entered. The end of a $\bar{W}$ controlled WRITE or $\bar{E}$ controlled WRITE is the end of an $\bar{E}$ controlled WRITE.

It is recommended that $\bar{E}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common $\bar{E}$ lines. $\bar{E}$ is left LOW internally only after the output buffers have been disabled.

NONVOLATILE STORE

The STK11C48 STORE cycle is initiated by executing a sequence of READ cycles from six specific addresses located by typing on READ cycles only the STK11C48 nonvolatile store addresses while remaining in the STORE state. During the STORE cycle, the data on pins D_0 through D_7 will be written into the memory if a valid cycle is entered. The end of a $\bar{W}$ controlled STORE or $\bar{E}$ controlled STORE is the end of an $\bar{E}$ controlled STORE.

ORDERING INFORMATION

STK11C48 - P 30 I

Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

30 = 30ns

35 = 35ns

45 = 45ns

Package

P = Plastic 28 pin 300 mil DIP

W = Plastic 28 pin 600 mil DIP

S = Plastic 28 pin SOIC

ORDERING INFORMATION

STK1108 - P. 00 1

Temperature Range

W = Commercial (-20 to 70 degrees C)
I = Industrial (-40 to 85 degrees C)

Access Time

20 - 30ns
30 - 35ns
45 - 55ns

Package

P = Plastic 28 pin 300 mil DIP
W = Plastic 28 pin 300 mil DIP
S = Plastic 28 pin SOIC

3



STK22C48

CMOS nvSRAM

2K x 8 High Performance

AutoStore™ Nonvolatile Static RAM

FEATURES

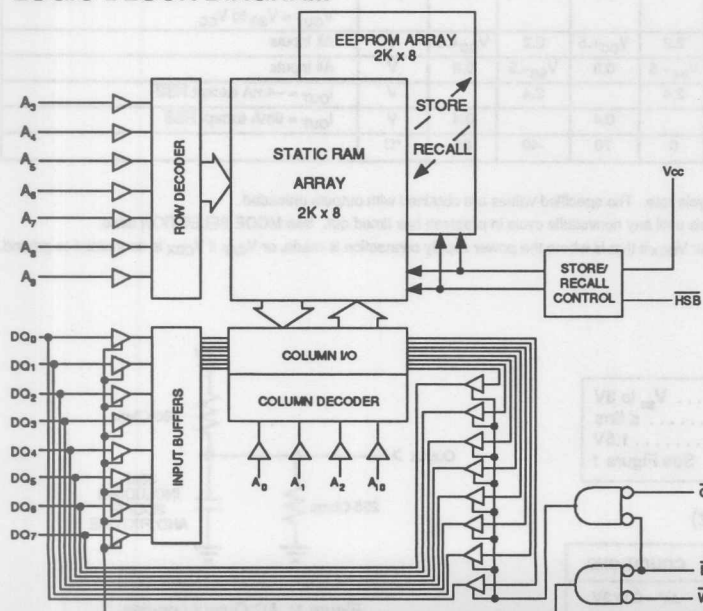
- 30, 35 and 45ns Access Times
- 15 mA I_{CC} at 200ns Access Speed
- Automatic *STORE* to EEPROM on Power Down
- Hardware Initiated *STORE* to EEPROM
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Unlimited *RECALL* cycles from EEPROM
- Single $5V \pm 10\%$ Operation
- Commercial and Industrial Temperatures
- Available in 28 pin 600-mil plastic DIP and 350-mil SOIC packages

DESCRIPTION

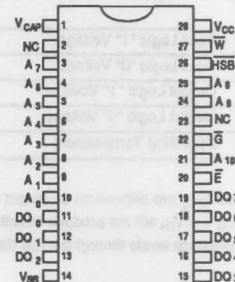
The Simtek STK22C48 is a fast static RAM (30, 35 and 45ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) take place automatically upon power down using charge stored in an external 100 μF capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on power up. A *STORE* can also be initiated via a single pin HSB.

3

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 600 PDIP
28 - 350 SOIC

PIN NAMES

A ₀ - A ₁₀	Address Inputs
W	Write Enable
DQ ₀ - DQ ₇	Data In/Out
E	Chip Enable
G	Output Enable
V _{CCX}	Power (+5V)
V _{SS}	Ground
V _{CAP}	Capacitor
HSB	Hardware Store/Busy

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS}	-0.6V to 7.0V
Voltage on $DQ_{0,7}$ and $\bar{Q}$	-0.5V to ($V_{CCX}+0.5V$)
Temperature under bias.....	-55°C to 125°C
Storage temperature.....	-65°C to 150°C
Power dissipation.....	1W
DC output current.....	15mA
(One output at a time, one second duration)	

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

$$(V_{CC} = 5.0V \pm 10\%)^d$$

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		85		95	mA	$t_{AVAV} = 30ns$
			80		85	mA	$t_{AVAV} = 35ns$
			75		80	mA	$t_{AVAV} = 45ns$
I_{CC2}	Average V_{CC} Current During STORE		6		7	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC3}^b	Average V_{CC} Current at $t_{AVAV} = 200ns$		15		15	mA	$\bar{E} \leq 0.2V, W \geq (V_{CC} - 0.2V)$
							others $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	Average V_{CC} current during AutoStore™		4		4	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		35		39	mA	$t_{AVAV} = 30ns$
			32		35	mA	$t_{AVAV} = 35ns$
			28		32	mA	$t_{AVAV} = 45ns$
							$\bar{E} \geq V_{IH}$; all others cycling
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\bar{E} \geq (V_{CC} - 0.2V)$
							all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK3}	Input Leakage Current (Any Input)		± 1		± 1	μA	$V_{CC} = \max$
							$V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5		± 5	μA	$V_{CC} = \max$
							$V_{OUT} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$ except HSB
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$ except HSB
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: V_{CC} reference levels throughout this datasheet refer to V_{CCX} if that is where the power supply connection is made, or V_{CAP} if V_{CCX} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels.....	V_{SS} to 3V
Input Rise and Fall Times.....	$\leq 5ns$
Input and Output Timing Reference Levels.....	1.5V
Output Load.....	See Figure 1

CAPACITANCE^e ($T_A=25^\circ C, f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IH}	Input Capacitance	8	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

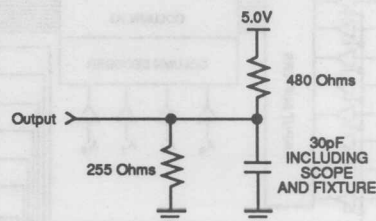


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

READ CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)^d$

NO.	SYMBOLS		PARAMETER	STK22C48-30		STK22C48-35		STK22C48-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELOV}	t_{ACS}	Chip Enable Access Time		30		35		45	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	30		35		45		ns
3	t_{AVOV}^g	t_{AA}	Address Access Time		30		35		45	ns
4	t_{GLOV}	t_{OE}	Output Enable to Data Valid		15		20		25	ns
5	t_{AXOX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELOX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHOZ}^h	t_{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t_{GLOX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHOZ}^h	t_{OHZ}	Output Disable to Output Inactive		15		17		20	ns
10	t_{ELICCH}^e	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{c,e}$	t_{PS}	Chip Disable to Power Standby		30		35		45	ns

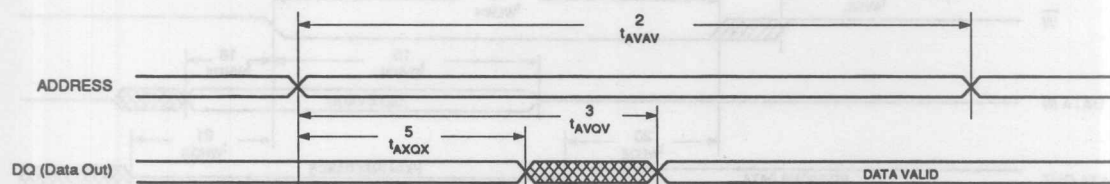
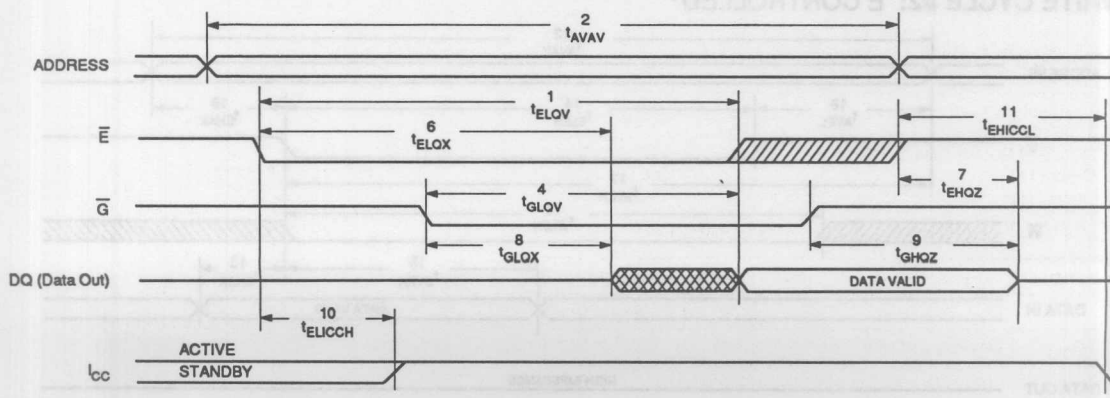
Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note e: Parameter guaranteed but not tested.

Note f: For READ CYCLE #1 and #2, $\bar{W}$ is high for entire cycle.

Note g: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note h: Measured $\pm 200mV$ from steady state output voltage.

READ CYCLE #1 ^{f,g}READ CYCLE #2 ^f

WRITE CYCLES #1 & #2

($V_{CC} = 5.0V \pm 10\%$)^d

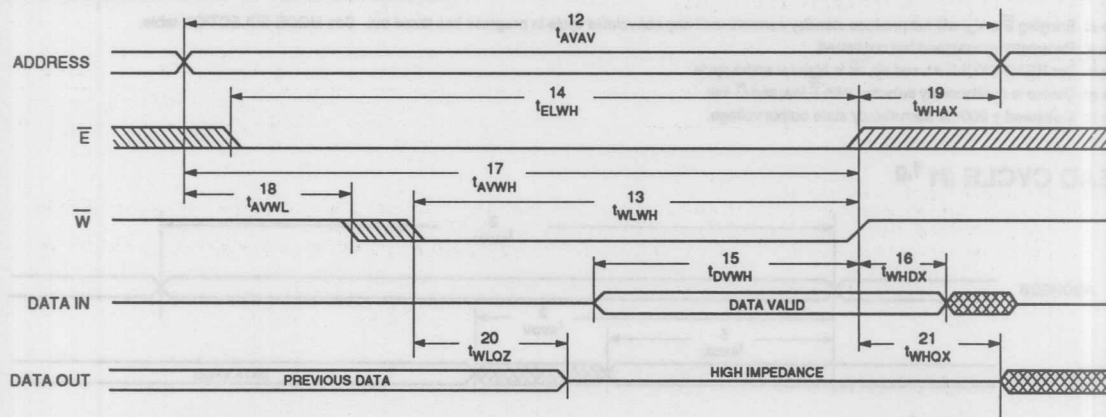
NO.	SYMBOLS			PARAMETER	STK22C48-30		STK22C48-35		STK22C48-45		UNITS
	#1	#2	AIL		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	30		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	25		30		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	25		30		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		18		20		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	25		30		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	$t_{WLOZ}^{h)}$		t_{WZ}	Write Enable to Output Disable		15		17		20	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note h: Measured $\pm 200mV$ from steady state output voltage.

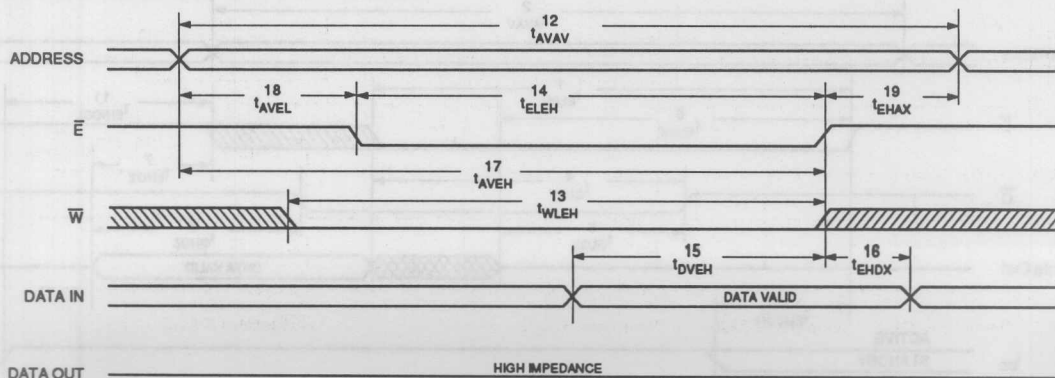
Note i: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ during address transitions.

Note j: If $\bar{W}$ is low when $\bar{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\bar{W}$ CONTROLLEDⁱ



WRITE CYCLE #2: $\bar{E}$ CONTROLLEDⁱ



NONVOLATILE MEMORY OPERATION

MODE SELECTION

E	W	HSB	A ₁₀ - A ₀ (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	STORE/Inhibit	Output High Z	I _{CC2} / Standby	k

Note k: HSB initiated *STORE* operation actually occurs only if a *WRITE* has been done since last *STORE* operation. After the *STORE* (if any) completes, the part will go into standby mode inhibiting all operation until HSB rises.

HARDWARE STORE / RECALL

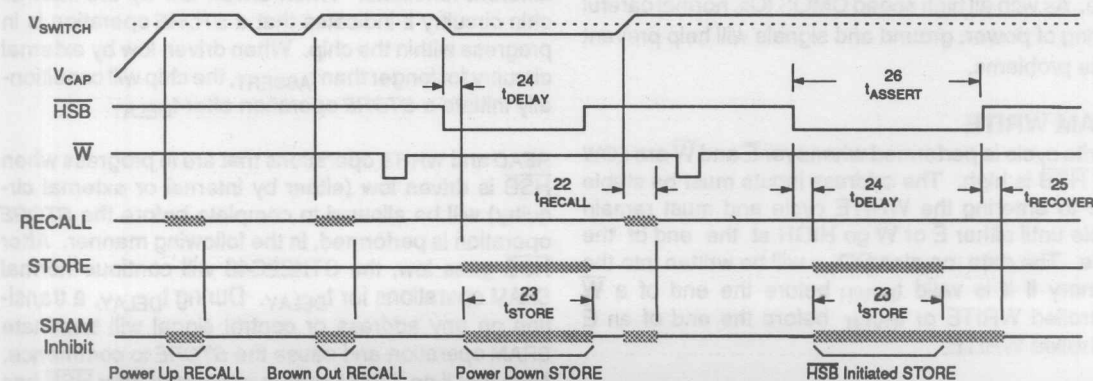
NO.	SYMBOLS	PARAMETER	MIN	MAX	UNITS	NOTES
22	t _{RECALL}	RECALL Cycle Duration		20	μs	Note m
23	t _{STORE} t _{HLHH}	STORE Cycle Duration		10	ms	V _{CC} ≥ 4.5V
24	t _{DELAY} t _{HLOZ}	HSB Low to Inhibit On	1		μs	
25	t _{RECOVER} t _{HHOX}	HSB High to Inhibit Off		300	ns	Note e
26	t _{ASSERT} t _{HLHX}	External STORE Pulse Width	250		ns	Note e
	V _{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
	I _{HSB_OL}	HSB Output Low Current	3		mA	HSB = V _{OL} , Note e, l
	I _{HSB_OH}	HSB Output High Current	5	60	μA	HSB = V _{IL} , Note e, l

Note e: These parameters guaranteed but not tested.

Note l: HSB is an I/O that has a weak internal pullup; it is basically an open drain output. It is meant to allow up to 32 STK22C48s to be ganged together for simultaneous storing. Do not use HSB to pullup any external circuitry other than other STK22C48 HSB pins.

Note m: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds V_{SWITCH}. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

HARDWARE STORE / RECALL



DEVICE OPERATION

The STK22C48 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via $\overline{\text{HSB}}$ assertion and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH} . *RECALL* operations are automatically initiated upon power-up and whenever the power supply voltage level rises above V_{SWITCH} .

SRAM READ

The STK22C48 performs a *READ* cycle whenever $\overline{\text{E}}$ and $\overline{\text{G}}$ are LOW and $\overline{\text{HSB}}$ and $\overline{\text{W}}$ are HIGH. The address specified on pins A_{0-10} determines which of the 2048 data bytes will be accessed. When the *READ* is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} . If the *READ* is initiated by $\overline{\text{E}}$ or $\overline{\text{G}}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later. The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{\text{E}}$ or $\overline{\text{G}}$ is brought HIGH or $\overline{\text{W}}$ or $\overline{\text{HSB}}$ is brought LOW.

NOISE CONSIDERATIONS

The STK22C48 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately $0.1\mu\text{F}$ connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\overline{\text{E}}$ and $\overline{\text{W}}$ are LOW and $\overline{\text{HSB}}$ is high. The address inputs must be stable prior to entering the *WRITE* cycle and must remain stable until either $\overline{\text{E}}$ or $\overline{\text{W}}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{\text{W}}$ controlled *WRITE* or t_{DVEH} before the end of an $\overline{\text{E}}$ controlled *WRITE*.

It is recommended that $\overline{\text{G}}$ be kept HIGH during the entire

WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{\text{G}}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{\text{W}}$ goes LOW.

AUTOMATIC RECALL

During power up, or after any low power condition ($V_{\text{CAP}} < V_{\text{SWITCH}}$), when V_{CAP} exceeds the sense voltage of V_{SWITCH} , a *RECALL* cycle will automatically be initiated. After the initiation of this automatic *RECALL*, if V_{CAP} falls below V_{SWITCH} , then another *RECALL* operation will be performed whenever V_{CAP} again rises above V_{SWITCH} .

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

If the STK22C48 is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{\text{W}}$ and system V_{CC} .

HARDWARE PROTECT

The STK22C48 offers hardware protection against inadvertent *STORE* operation during low voltage conditions. When $V_{\text{CAP}} < V_{\text{SWITCH}}$, $\overline{\text{HSB}}$ initiated *STORE* operations will be inhibited.

HSB OPERATION

The Hardware Store Busy pin ($\overline{\text{HSB}}$) is an open drain circuit acting as both input and output to perform two different functions. When driven low by the internal chip circuitry it indicates that a *STORE* operation is in progress within the chip. When driven low by external circuitry for longer than t_{ASSERT} , the chip will conditionally initiate a *STORE* operation after t_{DELAY} .

READ and *WRITE* operations that are in progress when $\overline{\text{HSB}}$ is driven low (either by internal or external circuitry) will be allowed to complete before the *STORE* operation is performed, in the following manner. After $\overline{\text{HSB}}$ goes low, the STK22C48 will continue normal SRAM operations for t_{DELAY} . During t_{DELAY} , a transition on any address or control signal will terminate SRAM operation and cause the *STORE* to commence. Note that if an SRAM write is attempted after $\overline{\text{HSB}}$ has

been forced low, the write will not occur and the *STORE* operation will begin immediately.

Hardware-Store-Busy ($\overline{\text{HSB}}$) is a high speed, low drive capability bi-directional control line. In order to allow a bank of STK22C48s to perform synchronized *STORE* functions, the $\overline{\text{HSB}}$ pin from a number of chips may be connected together. Each chip contains a small internal current source to pull $\overline{\text{HSB}}$ HIGH when it is not being driven low. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to V_{CC} via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed $I_{\text{HSB_OL}}$ at V_{OL} . Do not connect this or any other pull-up to the V_{CAP} node.

If $\overline{\text{HSB}}$ is to be connected to external circuits other than other STK22C48s, an external pull-up resistor should be used.

During any *STORE* operation, regardless of how it was initiated, the STK22C48 will continue to drive the $\overline{\text{HSB}}$ pin low, releasing it only when the *STORE* is complete. Upon completion of a *STORE* operation, the part will be disabled until $\overline{\text{HSB}}$ actually goes HIGH.

AUTOMATIC STORE OPERATION

During normal operation, the STK22C48 will draw current from V_{CC} to charge up a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. When the voltage on the V_{CAP} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CC} and initiate a *STORE* operation.

Figure 1 shows the proper connection of capacitors for automatic store operation. The charge storage capacitor should have a capacity of at least 100 μF ($\pm 20\%$) at 6V. Each STK22C48 must have its own 100 μF capacitor. Each STK22C48 *must* have a high quality, high frequency bypass capacitor of 0.1 μF connected between V_{CAP} and V_{SS} , using leads and traces that are as short as possible.

If the AutoStore™ function is not required, then V_{CAP} should be tied directly to the power supply and V_{CC} should be tied to ground. In this mode, *STORE* operations may be triggered with the $\overline{\text{HSB}}$ pin. V_{CAP} (Pin 1) *must* always have a proper bypass capacitor connected to it.

In order to prevent unneeded *STORE* operations, automatic *STOREs* as well as those initiated by externally driving $\overline{\text{HSB}}$ LOW will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* cycle. Note that if $\overline{\text{HSB}}$ is driven low via external circuitry and no WRITES have taken place, the part will still be disabled until $\overline{\text{HSB}}$ is allowed to return HIGH.

PREVENTING AUTOMATIC STORES

The AutoStore™ function can be disabled on the fly by holding $\overline{\text{HSB}}$ HIGH with a driver capable of sourcing 15mA at a V_{OH} of at least 2.2V as it will have to overpower the internal pull-down device that drives $\overline{\text{HSB}}$ low for 50ns at the onset of an AutoStore™. When the STK22C48 is connected for AutoStore™ operation (system V_{CC} connected to V_{CC} and a 100 μF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK22C48 will attempt to pull $\overline{\text{HSB}}$ low; if $\overline{\text{HSB}}$ doesn't actually get below V_{IL} , the part will stop trying to pull $\overline{\text{HSB}}$ LOW and abort the AutoStore™ attempt.

LOW AVERAGE ACTIVE POWER

The STK22C48 has been designed to draw significantly less power when $\overline{\text{E}}$ is LOW (chip enabled) but the access cycle time is longer than 55ns. Figure 2 below shows the relationship between I_{CC} and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels, over the commercial temperature range. Figure 3 shows the same relationship for WRITE cycles. When $\overline{\text{E}}$ is HIGH, the chip consumes only standby currents, and these plots do not apply.

The cycle time used in Figure 2 corresponds to the length of time from the later of the last address transition or $\overline{\text{E}}$ going LOW to the earlier of $\overline{\text{E}}$ going HIGH or the next address transition. $\overline{\text{W}}$ is assumed to be HIGH, while the state of $\overline{\text{G}}$ does not matter. Additional current is consumed when the address lines change state while $\overline{\text{E}}$ is asserted. The cycle time used in Figure 3 corresponds to the length of time from the later of $\overline{\text{W}}$ or $\overline{\text{E}}$ going LOW to the earlier of $\overline{\text{W}}$ or $\overline{\text{E}}$ going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled ($\overline{\text{E}}$ HIGH); 3) the cycle time for accesses ($\overline{\text{E}}$ LOW); 4) the ratio of reads to writes; 5) the operating temperature and; 6) the V_{CC} level.

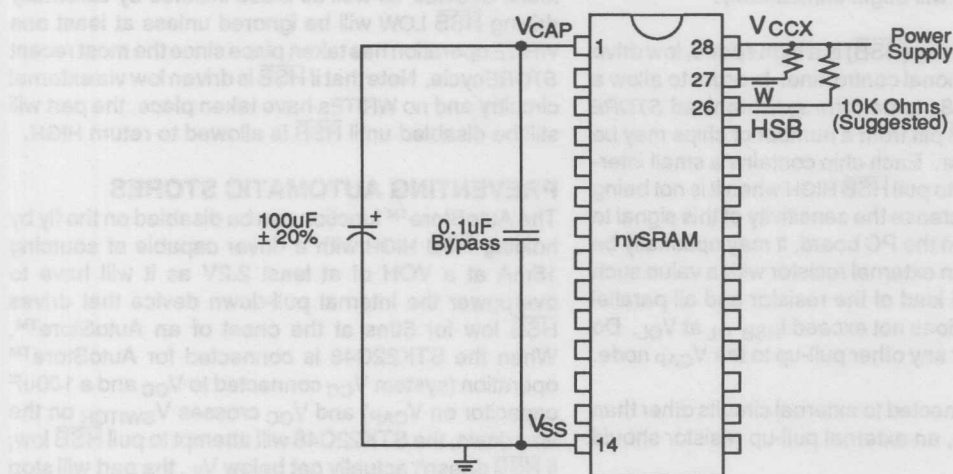


Figure 1. Schematic Diagram

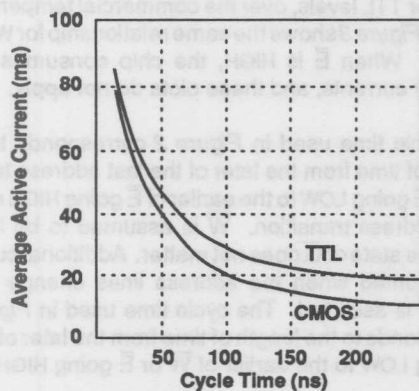


Figure 2. I_{CC} (Max) Reads

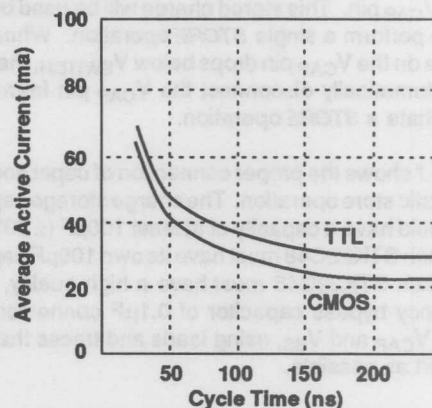


Figure 3. I_{CC} (Max) Writes

Note: Typical at 25° C

ORDERING INFORMATION

STK22C48 - W 35 I

Temperature Range

blank = Commercial (0 - 70 degrees C)

I = Industrial (-40 - 85 degrees C)

Access Time

30 = 30ns

35 = 35ns

45 = 45ns

Package

W= Plastic 28 pin 600-mil DIP

S = Plastic 28 pin 350-mil SOIC

3

NOTES

ORDERING INFORMATION

STK3202 - W 32

Temperature Range

Blank - Commercial (0 - 70 degrees C)
I - Industrial (-40 - 95 degrees C)

Access Time

30 = 30ns
35 = 35ns
45 = 45ns

Package

W - Plastic 28 pin 500-mil DIP
S - Plastic 28 pin 520-mil SOIC

3



SIMTEK

STK25C48

CMOS nvSRAM

2K x 8 High Performance
AutoStore™ Nonvolatile Static RAM

FEATURES

- 30, 35 and 45ns Access Times
- 15 mA I_{CC} at 200ns Access Speed
- Automatic *STORE* to EEPROM on Power Down
- Unlimited SRAM Read and Write Cycles
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Unlimited *RECALL* cycles from EEPROM
- Single $5V \pm 10\%$ Operation
- Commercial and Industrial Temperatures

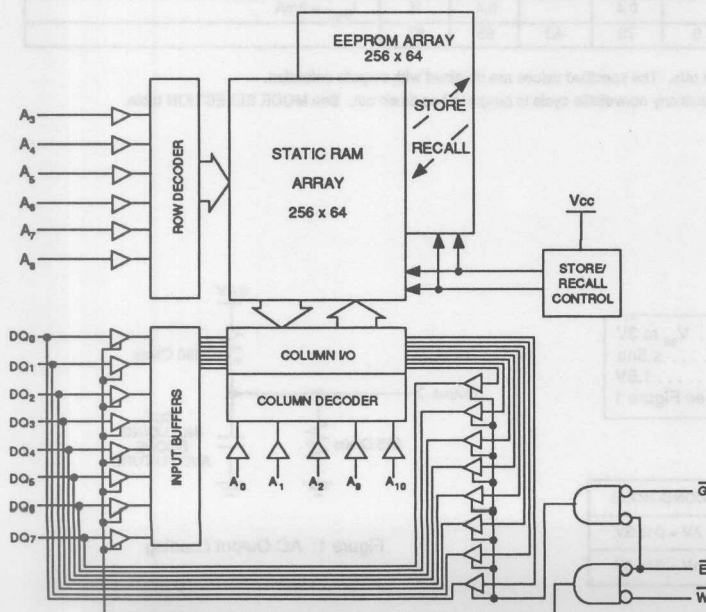
DESCRIPTION

The Simtek STK25C48 is a fast static RAM (30, 35 and 45ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) take place automatically upon power down. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on power up.

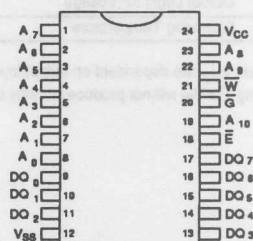
The STK25C48 is available in a 24-pin 600 mil plastic DIP package.

3

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



24 - 600 PDIP

PIN NAMES

$A_0 - A_{10}$	Address Inputs
W	Write Enable
$DQ_0 - DQ_7$	Data In/Out
E	Chip Enable
G	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS} -0.6V to 7.0V
Voltage on DQ₀₋₇ and $\bar{G}$ -0.5V to ($V_{CC}+0.5$)V
Temperature under bias -55°C to 125°C
Storage temperature -65°C to 150°C
Power dissipation 1W
DC output current 15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		85 80 75		95 85 80	mA	$t_{AVAV} = 30ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$
I_{CC2}^b	Average V_{CC} Current at $t_{AVAV} = 200ns$		15		15	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC3}	Average V_{CC} Current during AutoStore™ Cycle		4		4	mA	$E \leq 0.2V, W \geq (V_{CC} - 0.2V)$ others $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		35 32 28		39 35 32	mA	$t_{AVAV} = 30ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ $E \geq V_{IH}$; all others cycling
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		3		3	mA	$E \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK3}	Input Leakage Current (Any Input)		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5		± 5	μA	$V_{CC} = \max$ $V_{OUT} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} and I_{CC2} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $E \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

AC TEST CONDITIONS

Input Pulse Levels V_{SS} to 3V
Input Rise and Fall Times $\leq 5ns$
Input and Output Timing Reference Levels 1.5V
Output Load See Figure 1

CAPACITANCE^d ($T_A=25^\circ C, f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note d: These parameters are guaranteed but not tested.

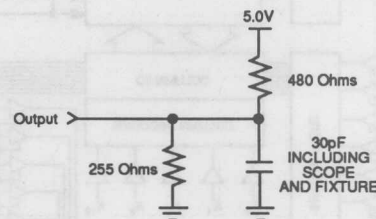


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

READ CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK25C48-30		STK25C48-35		STK25C48-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELOV}	t_{ACS}	Chip Enable Access Time		30		35		45	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	30		35		45		ns
3	t_{AVOV}^g	t_{AA}	Address Access Time		30		35		45	ns
4	t_{GLOV}	t_{OE}	Output Enable to Data Valid		15		20		25	ns
5	t_{AXOX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELOX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHOZ}^h	t_{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t_{GLOX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHOZ}^h	t_{OHZ}	Output Disable to Output Inactive		15		17		20	ns
10	t_{ELICCH}^g	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}^g	t_{PS}	Chip Disable to Power Standby		30		35		45	ns

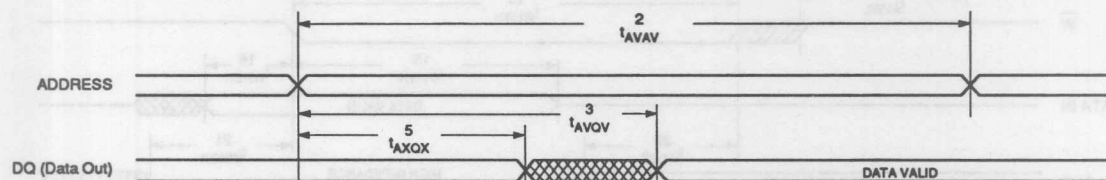
Note e: Parameter guaranteed but not tested.

Note f: For READ CYCLE #1 and #2, $\overline{W}$ is high for entire cycle.

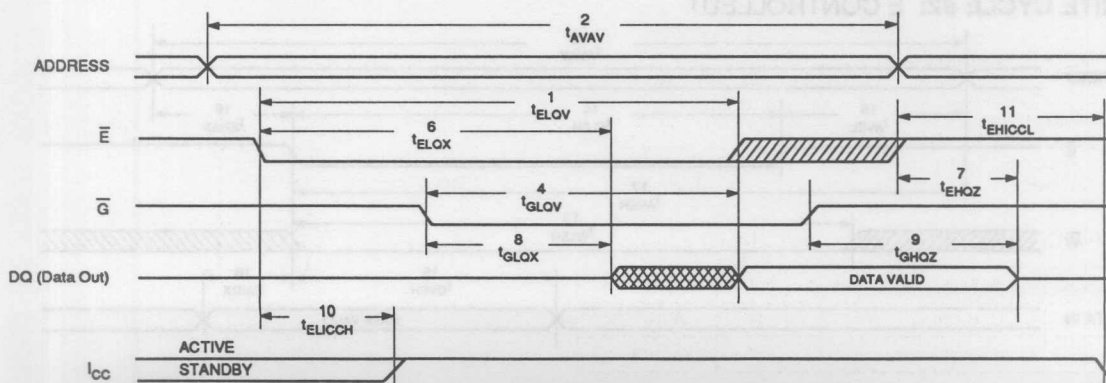
Note g: Device is continuously selected with $\overline{E}$ low and $\overline{G}$ low.

Note h: Measured $\pm 200mV$ from steady state output voltage.

READ CYCLE #1 g,h



READ CYCLE #2 g

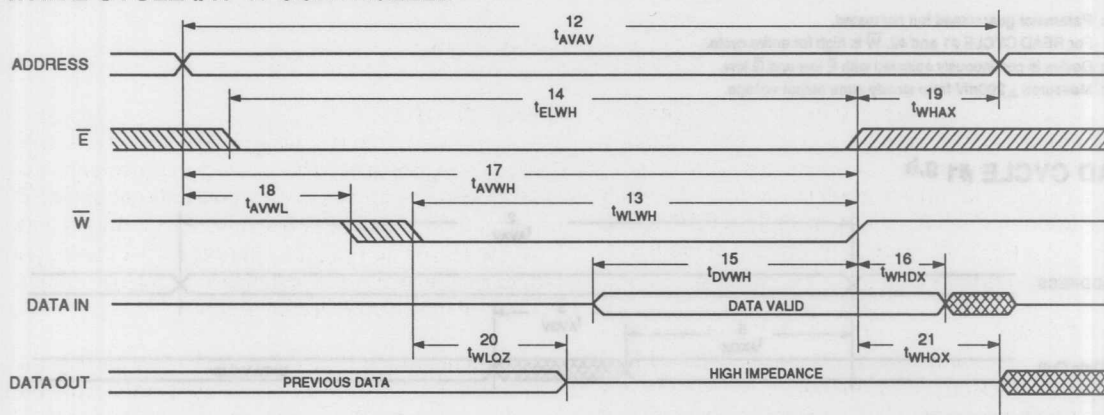
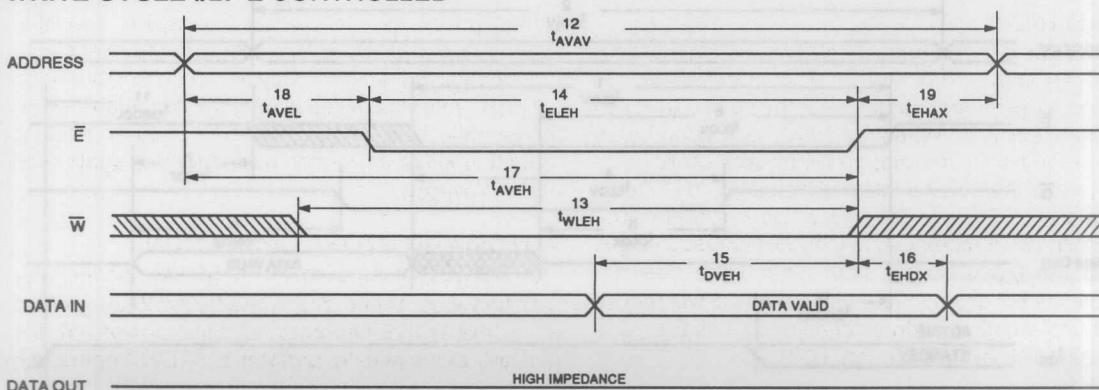


WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	STK25C48-30		STK25C48-35		STK25C48-45		UNITS
	#1	#2	AJL		MIN	MAX	MIN	MAX	MIN	MAX	
12	t _{AVAV}	t _{AVAV}	t _{WC}	Write Cycle Time	30		35		45		ns
13	t _{WLWH}	t _{WLEH}	t _{WP}	Write Pulse Width	25		30		35		ns
14	t _{ELWH}	t _{ELEH}	t _{CW}	Chip Enable to End of Write	25		30		35		ns
15	t _{DVWH}	t _{DVEH}	t _{DW}	Data Set-up to End of Write	15		18		20		ns
16	t _{WHDX}	t _{EHDH}	t _{DH}	Data Hold After End of Write	0		0		0		ns
17	t _{AVWH}	t _{AVEH}	t _{AW}	Address Set-up to End of Write	25		30		35		ns
18	t _{AVWL}	t _{AVEL}	t _{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t _{WHAX}	t _{EHAX}	t _{WR}	Address Hold After End of Write	0		0		0		ns
20	t _{WLOZ} ^h		t _{WZ}	Write Enable to Output Disable		15		17		20	ns

Note h: Measured ±200mV from steady state output voltage.

Note i: $\bar{E}$ or $\bar{W}$ must be ≥ V_{IH} during address transitions.Note j: If $\bar{W}$ is low when $\bar{E}$ goes low, the outputs remain in the high impedance state.WRITE CYCLE #1: $\bar{W}$ CONTROLLED^jWRITE CYCLE #2: $\bar{E}$ CONTROLLED^j

NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	I/O	POWER
H	X	X	Not Selected	Output High Z	Standby
L	H	L	Read SRAM	Output Data	Active
L	L	X	Write SRAM	Input Data	Active
L	H	H	No Operation	High Z	Active

AUTOSTORE™ AND POWER-UP RECALL

NO.	SYMBOLS	PARAMETER	MIN	MAX	UNITS	NOTES
22	t_{RECALL}	RECALL Cycle Duration		20	μs	Note k
23	t_{PDSTORE}	Power Down STORE Duration		10	ms	
	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	

Note k: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds V_{SWITCH} . t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

DEVICE OPERATION

The STK25C48 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

STORE cycles are automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH} . *RECALL* operations are automatically initiated upon power-up and whenever the power supply voltage level rises above V_{SWITCH} .

SRAM READ

The STK25C48 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ is HIGH. The address specified on pins A_0 - A_{10} determines which of the 2048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} . If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or t_{GLQV} , whichever is later. The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_0 - DQ_7 will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes LOW.

During power-up, or after any low power condition ($V_{\text{CC}} < V_{\text{SWITCH}}$), when V_{CC} exceeds the sense voltage of V_{SWITCH} , a *RECALL* cycle will automatically be initiated. After the initiation of this automatic *RECALL*, if V_{CC} falls below V_{SWITCH} , then another *RECALL* operation will be performed whenever V_{CC} again rises above V_{SWITCH} .

AUTOMATIC STORE OPERATION

The STK25C48 AutoStore™ nvSRAM continuously monitors V_{CC} . When V_{CC} drops below V_{SWITCH} (and an SRAM WRITE has occurred since power-up), the part will automatically perform a *STORE* operation,

saving the data into the EEPROM. *Figure 1* illustrates the timing of the *AutoStore™* cycle. V_{CC} to the STK25C48 must not fall below 3.6V before the *AutoStore™* cycle is complete (t_{STORE}). In order to prevent unneeded STORE operations, automatic STORE will not occur unless at least one WRITE operation has taken place since power-up.

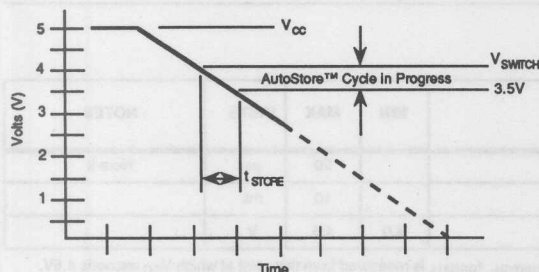


Figure 1
AutoStore™ Cycle Timing Diagram

Note: On power-up, as soon as the STK25C48 completes the power-up recall, it becomes an SRAM; if $\bar{E}$ and $\bar{W}$ are both low the address on the inputs will be written to, corrupting the recalled data. If V_{CC} bounces below V_{SWITCH} , the part will *AutoStore™* this corrupted SRAM data.

IMPLEMENTATION

Normally, the STK25C48 relies on the system V_{CC} remaining between V_{SWITCH} (min) and 3.6V for the STORE time, t_{STORE} . In the unusual case that the system power supply decays too quickly (not remaining between V_{SWITCH} (min) and 3.6V for at least 10ms), a possible alternative implementation is shown in *Figure 2*. The capacitor charge will hold up the DUT V_{CC} long enough for the *AutoStore™* to occur. However, from a system point of view, the 0.3V drop across

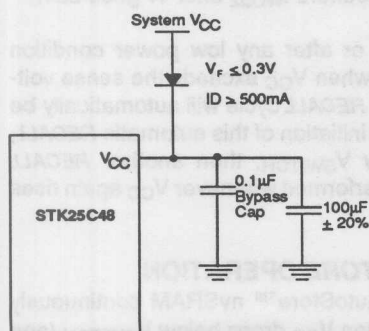


Figure 2
Alternate AutoStore™ Implementation Circuit if V_{CC} decays too quickly

the diode will effectively cause the V_{SWITCH} value to be 0.3V higher; the part could do an *AutoStore™* when the system V_{CC} is as high as $V_{SWITCH}(\text{max}) + 0.3V$. Note that the STK25C48 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1µF connected between DUT V_{CC} and V_{SS} , using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

LOW AVERAGE ACTIVE POWER

The STK25C48 has been designed to draw significantly less power when $\bar{E}$ is LOW (chip enabled) but the access cycle time is longer than 55ns. *Figure 3* below shows the relationship between I_{CC} and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels, over the commercial temperature range. *Figure 4* shows the same relationship for WRITE cycles. When $\bar{E}$ is HIGH, the chip consumes only standby currents and these plots do not apply.

The cycle time used in *Figure 3* corresponds to the length of time from the later of the last address transition or $\bar{E}$ going LOW to the earlier of $\bar{E}$ going HIGH or the next address transition. $\bar{W}$ is assumed to be HIGH, while the state of $\bar{G}$ does not matter. Additional current is consumed when the address lines change state while $\bar{E}$ is asserted. The cycle time used in *Figure 4* corresponds to the length of time from the later of $\bar{W}$ or $\bar{E}$ going LOW to the earlier of $\bar{W}$ or $\bar{E}$ going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled ($\bar{E}$ HIGH); 3) the cycle time for accesses ($\bar{E}$ LOW); 4) the ratio of reads to writes; 5) the operating temperature and; 6) the V_{CC} level.

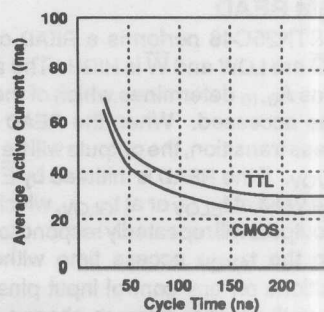
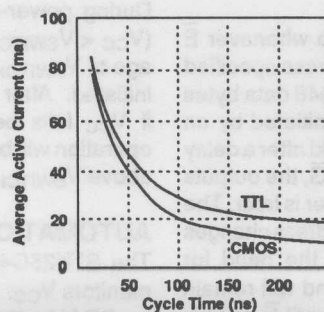


Figure 4
 $I_{CC}(\text{Max})$ Writes

Note: Typical at 25°C

ORDERING INFORMATION

STK25C48 - W 30 I

Temperature Range

blank = Commercial (0 - 70 degrees C)

I = Industrial (-40 - 85 degrees C)

Access Time

30 = 30ns

35 = 35ns

45 = 45ns

Package

W= Plastic 24 pin 600 mil DIP

3

64 kilobit nvSRAM Products 4



STK10C68

CMOS nvSRAM

High Performance

8K x 8 Nonvolatile Static RAM

FEATURES

- 25, 30, 35 and 45ns Access Times
- 12, 15, 20 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Hardware *STORE* Initiation
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Hardware *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single 5V±10% Operation
- Commercial and Industrial Temperatures
- Available in multiple standard packages

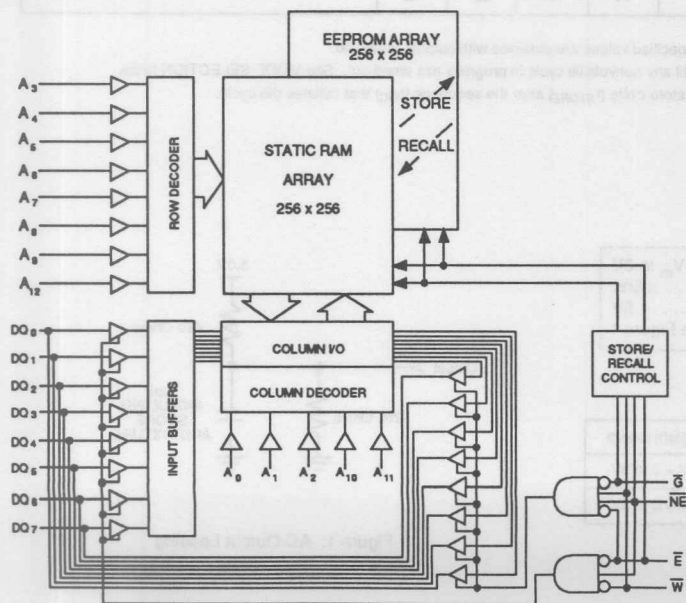
DESCRIPTION

The Simtek STK10C68 is a fast static RAM (25, 30, 35, and 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) using the $\overline{NE}$ pin. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

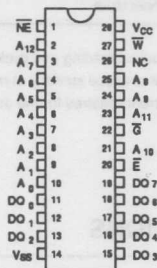
The STK10C68 features industry standard pinout for nonvolatile RAMs in a 28-pin 300 mil plastic or ceramic DIP, and a 28-pin SOIC package. MIL-STD-883 and Standard Military Drawing (SMD #5962-93056) devices are also available.

4

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 300 PDIP
28 - 300 CDIP
28 - 350 SOIC

PIN NAMES

A ₀ - A ₁₂	Address Inputs
$\overline{W}$	Write Enable
DQ ₀ - DQ ₇	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS} -0.6V to 7.0V
 Voltage on DQ₀₋₇ and $\bar{G}$ -0.5V to ($V_{CC}+0.5V$)
 Temperature under bias -55°C to 125°C
 Storage temperature -65°C to 150°C
 Power dissipation 1W
 DC output current 15mA
 (One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		90		95	mA	$t_{AVAV} = 25ns$
			85		90	mA	$t_{AVAV} = 30ns$
			80		85	mA	$t_{AVAV} = 35ns$
			75		80	mA	$t_{AVAV} = 45ns$
I_{CC2}^d	Average V_{CC} Current during STORE cycle		50		50	mA	$E \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30		34	mA	$t_{AVAV} = 25ns$
			27		30	mA	$t_{AVAV} = 30ns$
			23		27	mA	$t_{AVAV} = 35ns$
			20		23	mA	$t_{AVAV} = 45ns$
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		1		1	mA	$E \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{LK}	Input Leakage Current (Any Input)		±1		±1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5		±5	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: I_{CC2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels V_{SS} to 3V
 Input Rise and Fall Times ≤ 5ns
 Input and Output Timing Reference Levels 1.5V
 Output Load See Figure 1

CAPACITANCE^e ($T_A=25^\circ C$, $f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

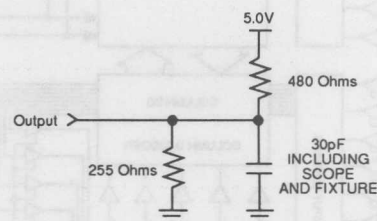


Figure 1: AC Output Loading

READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK10C68-25		STK10C68-30		STK10C68-35		STK10C68-45		UNITS
	#1, #2	AIL		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t _{ELOV}	t _{ACS}	Chip Enable Access Time		25		30		35		45	ns
2	t _{AVAV} ^g	t _{RC}	Read Cycle Time	25		30		35		45		ns
3	t _{AVOV} ^h	t _{AA}	Address Access Time		25		30		35		45	ns
4	t _{GLOV}	t _{OE}	Output Enable to Data Valid		12		15		20		25	ns
5	t _{AXOX}	t _{OH}	Output Hold After Address Change	5		5		5		5		ns
6	t _{ELOX}	t _{LZ}	Chip Enable to Output Active	5		5		5		5		ns
7	t _{EHQZ} ⁱ	t _{HZ}	Chip Disable to Output Inactive		13		15		17		20	ns
8	t _{GLOX}	t _{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t _{GHOZ} ⁱ	t _{OHZ}	Output Disable to Output Inactive		13		15		17		20	ns
10	t _{ELICCH} ^e	t _{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t _{EHICCL} ^{c,e}	t _{PS}	Chip Disable to Power Standby		25		30		35		45	ns
11A	t _{WHOV}	t _{WR}	Write Recovery Time		30		35		45		55	ns

Note c: Bringing $\bar{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note e: Parameter guaranteed but not tested.

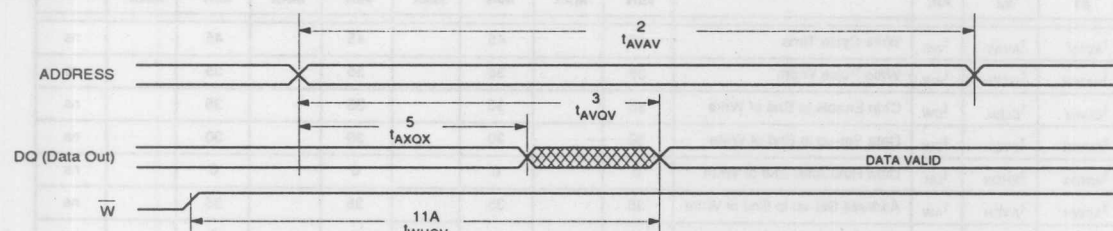
Note f: $\bar{NE}$ must be high during entire cycle.

Note g: For READ CYCLE #1 and #2, $\bar{W}$ and $\bar{NE}$ must be high for entire cycle.

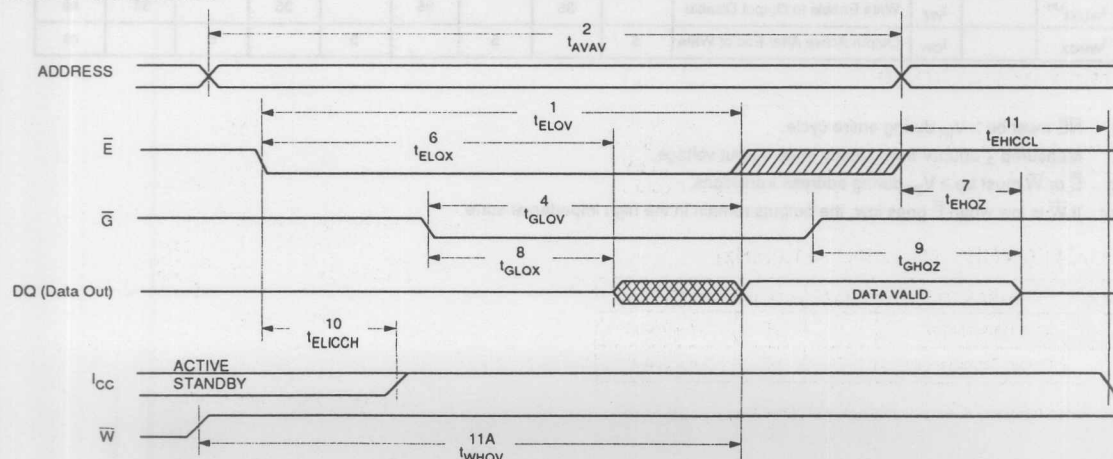
Note h: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note i: Measured ± 200mV from steady state output voltage.

READ CYCLE #1 f,g,h



READ CYCLE #2 f,g



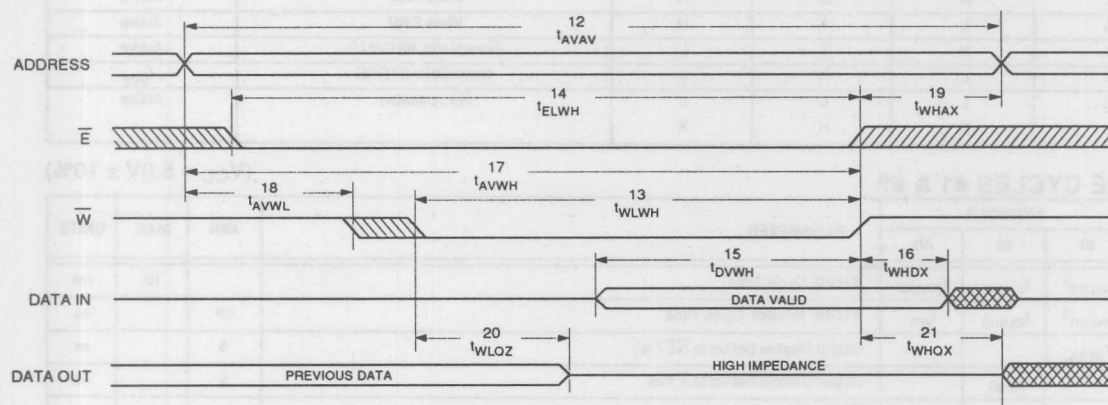
WRITE CYCLES #1 & #2; $\bar{G}$ high $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	STK10C68-25		STK10C68-30		STK10C68-35		STK10C68-45		UNITS
	#1	#2	Ail		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		30		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	12		15		18		20		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns

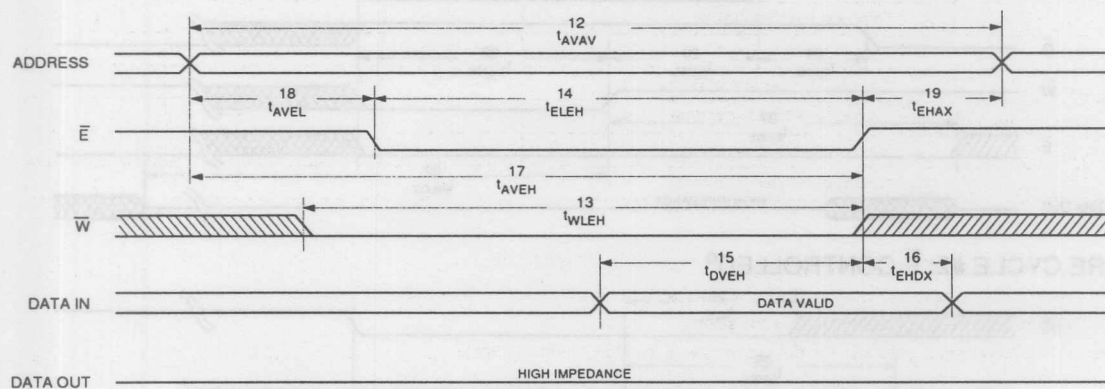
WRITE CYCLES #1 & #2; $\bar{G}$ low $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	STK10C68-25		STK10C68-30		STK10C68-35		STK10C68-45		UNITS
	#1	#2	Ail		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	45		45		45		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	35		35		35		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	35		35		35		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	30		30		30		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	35		35		35		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns
20	$t_{WLOZ}^{l,m}$		t_{WZ}	Write Enable to Output Disable		35		35		35		35	ns
21	t_{WHOX}		t_{OW}	Output Active After End of Write	5		5		5		5		ns

Note f: $\bar{NE}$ must be $\geq V_{IH}$ during entire cycle.Note i: Measured $\pm 200mV$ from steady state output voltage.Note k: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ during address transitions.Note m: If $\bar{W}$ is low when $\bar{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\overline{W}$ CONTROLLED^{f,k}

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WRITE CYCLE #2: $\overline{E}$ CONTROLLED^{f,k}

NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\bar{E}$	$\bar{W}$	$\bar{G}$	$\bar{NE}$	MODE	POWER
H	X	X	X	Not Selected	Standby
L	H	L	H	Read RAM	Active
L	L	X	H	Write RAM	Active
L	H	L	L	Nonvolatile <i>RECALL</i> ⁿ	Active
L	L	H	L	Nonvolatile <i>STORE</i>	I_{CC2}
L	L	L	L	No operation	Active
L	H	H	X		

STORE CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt.				
22	t_{WLOX}^p	t_{ELOXS}	t_{STORE}	STORE Cycle Time		10	ms
23	t_{WLNH}^q	t_{ELNHS}	t_{WC}	STORE Initiation Cycle Time	25		ns
24	t_{GHNH}			Output Disable Set-up to $\bar{NE}$ Fall	5		ns
25		t_{GHFL}		Output Disable Set-up to $\bar{E}$ Fall	5		ns
26	t_{NLWL}	t_{NLEL}		$\bar{NE}$ Set-up	5		ns
27	t_{ELWL}			Chip Enable Set-up	5		ns
28		t_{WLEL}		Write Enable Set-up	5		ns

Note n: An automatic *RECALL* also takes place at power up, starting when V_{CC} exceeds 4.0V, and taking t_{RECALL} from the time at which V_{CC} exceeds 4.5V.

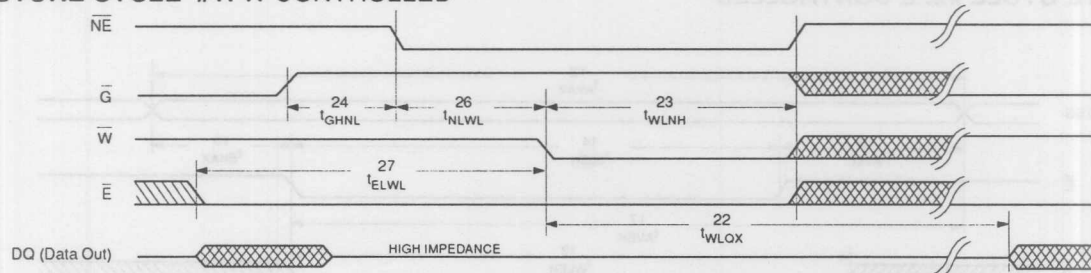
V_{CC} must not drop below 4.0V once it has been exceeded for the *RECALL* to function properly.

Note o: If $\bar{E}$ is low for any period of time in which $\bar{W}$ is high while $\bar{G}$ and $\bar{NE}$ are low, then a *RECALL* cycle may be initiated.

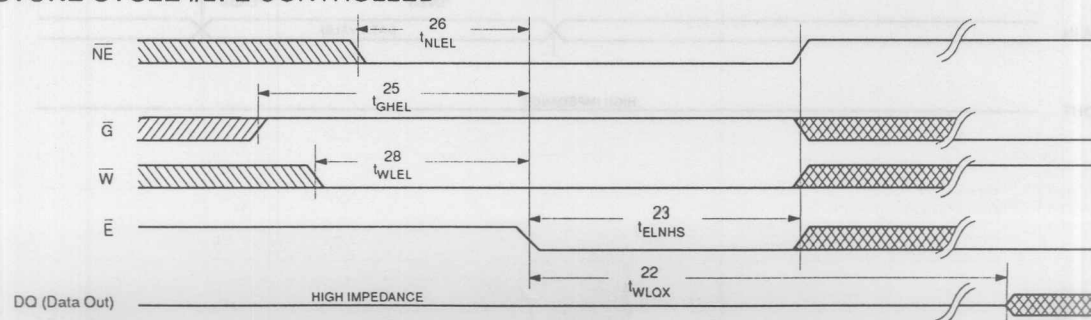
Note p: Measured with $\bar{W}$ and $\bar{NE}$ both returned high, and $\bar{G}$ returned low. Note that *STORE* cycles are inhibited/aborted by $V_{CC} < 4.0V$ (*STORE* inhibit).

Note q: Once t_{WC} has been satisfied by $\bar{NE}$, $\bar{G}$, $\bar{W}$ and $\bar{E}$, the *STORE* cycle is completed automatically. Any of $\bar{NE}$, $\bar{G}$, $\bar{W}$ or $\bar{E}$ may be used to terminate the *STORE* initiation cycle.

STORE CYCLE #1: $\bar{W}$ CONTROLLED^o



STORE CYCLE #2: $\bar{E}$ CONTROLLED^o



RECALL CYCLES #1, #2 & #3

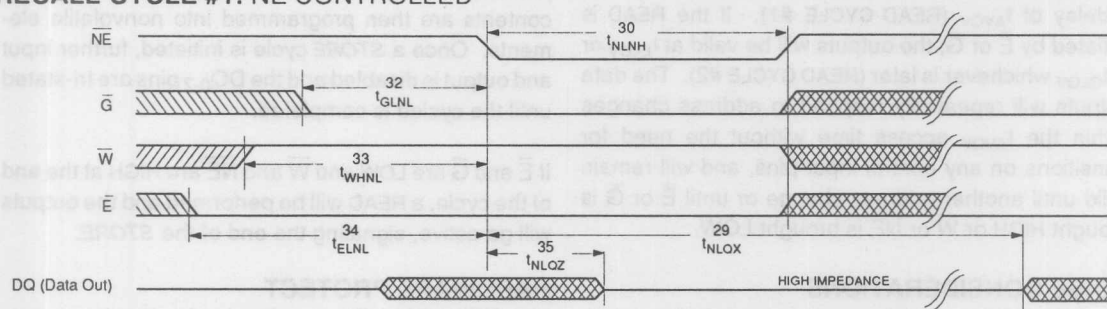
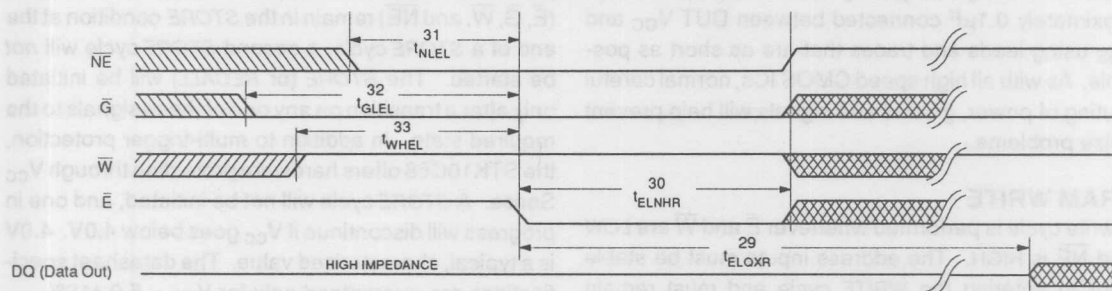
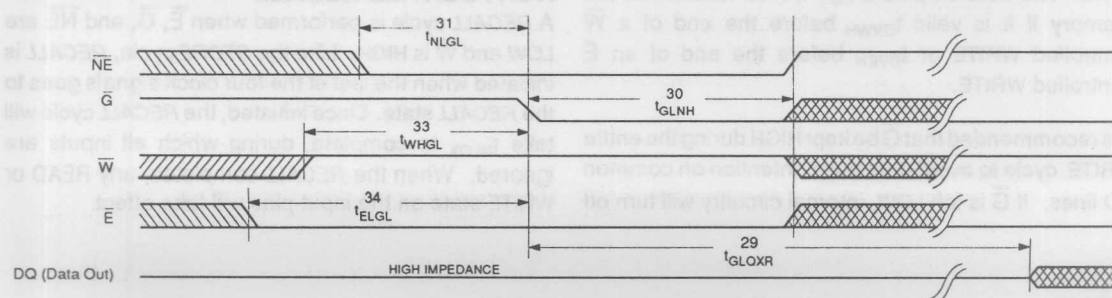
(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	#3				
29	t _{NLOX} ¹	t _{ELOXR}	t _{GLOXR}	RECALL Cycle Time		20	μs
30	t _{NLNH} ⁵	t _{ELNHR}	t _{GLNH}	RECALL Initiation Cycle Time	25		ns
31		t _{NLEL}	t _{NLGL}	$\overline{NE}$ Set-up	5		ns
32	t _{GLNL}	t _{GLEL}		Output Enable Set-up	5		ns
33	t _{WHNL}	t _{WHEL}	t _{WHGL}	Write Enable Set-up	5		ns
34	t _{ELNL}		t _{ELGL}	Chip Enable Set-up	5		ns
35	t _{NLOZ}			$\overline{NE}$ Fall to Outputs Inactive		25	ns

Note r: Measured with $\overline{W}$ and $\overline{NE}$ both high, and $\overline{G}$ and $\overline{E}$ low.

Note s: Once t_{NLNH} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the *RECALL* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$ or $\overline{E}$ may be used to terminate the *RECALL* initiation cycle.

Note t: If $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ is high, then a *STORE* cycle will be initiated instead of a *RECALL*.

RECALL CYCLE #1: $\overline{NE}$ CONTROLLED^oRECALL CYCLE #2: $\overline{E}$ CONTROLLED^oRECALL CYCLE #3: $\overline{G}$ CONTROLLED^{o,t}

DEVICE OPERATION

The STK10C68 has two modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pin. When in SRAM mode, the memory operates as a standard fast static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

SRAM READ

The STK10C68 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{NE}$ and $\overline{W}$ are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{NE}$ is brought LOW.

NOISE CONSIDERATIONS

The STK10C68 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately $0.1\mu F$ connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off

the output buffers t_{WLOZ} after $\overline{W}$ goes LOW.

Keeping $\overline{G}$ high during write cycles also enables use of the faster write specifications.

NONVOLATILE STORE

A STORE cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are LOW and $\overline{G}$ is HIGH. While any sequence to achieve this state will initiate a STORE, only $\overline{W}$ initiation (STORE CYCLE #1) and $\overline{E}$ initiation (STORE CYCLE #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a STORE cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a STORE cycle is initiated, further input and output is disabled and the DQ_{0-7} pins are tri-stated until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the STORE.

HARDWARE PROTECT

The STK10C68 offers two levels of protection to suppress inadvertent STORE cycles. If the control signals ($\overline{E}$, $\overline{G}$, $\overline{W}$, and $\overline{NE}$) remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will not be started. The STORE (or RECALL) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the STK10C68 offers hardware protection through V_{CC} Sense. A STORE cycle will not be initiated, and one in progress will discontinue if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC} = 5.0 \pm 10\%$.

NONVOLATILE RECALL

A RECALL cycle is performed when $\overline{E}$, $\overline{G}$, and $\overline{NE}$ are LOW and $\overline{W}$ is HIGH. Like the STORE cycle, RECALL is initiated when the last of the four clock signals goes to the RECALL state. Once initiated, the RECALL cycle will take t_{NLQX} to complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pins will take effect.

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the *STORE* cycle, a transition must occur on some control pin to cause a recall, preventing inadvertent multi-triggering. On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.0V, a *RECALL* cycle is automati-

cally initiated. The voltage on the V_{CC} pin must not drop below 4.0V once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{NLOX} after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK10C68 is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\bar{W}$ and system V_{CC} .

ORDERING INFORMATION

STK10C68 - P 30 I

Temperature Range

blank = Commercial (0 to 70 degrees C)
I = Industrial (-40 to 85 degrees C)

Access Time

25 = 25ns
30 = 30ns
35 = 35ns
45 = 45ns

Package

P = Plastic 28 pin 300 mil DIP
S = Plastic 28 pin SOIC
C = Ceramic 28 pin 300 mil DIP



STK10C68-M

CMOS nvSRAM

High Performance

8K x 8 Nonvolatile Static RAM

MIL-STD-833/SMD 5962 - 93056

FEATURES

- 35, 45 and 55ns Access Times
- 20 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Hardware *STORE* Initiation
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Hardware *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single 5V±10% Operation
- Available in multiple standard packages

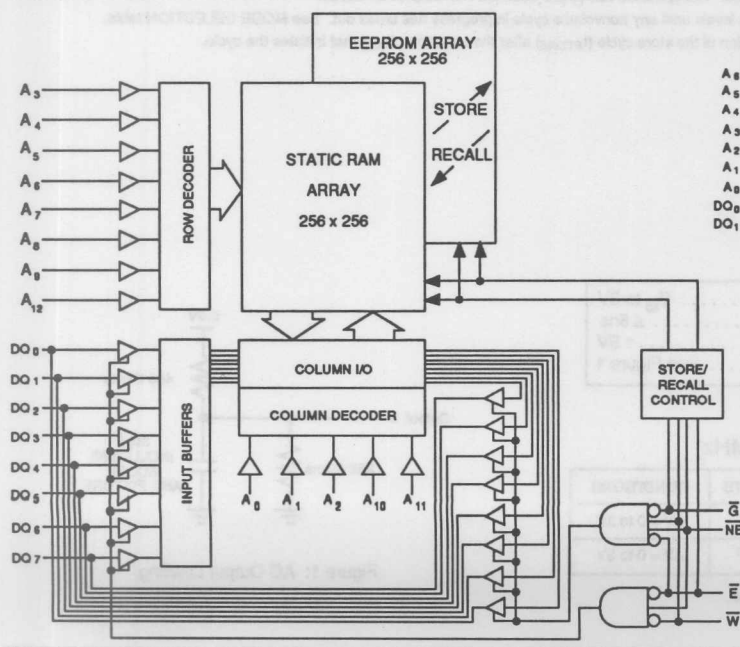
DESCRIPTION

The Simtek STK10C68-M is a fast static RAM (35, 45 and 55ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) using the NE pin. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

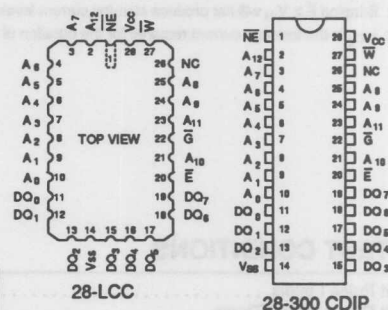
The STK10C68 features industry standard pinout for nonvolatile RAMs in a 28-pin 300 mil ceramic DIP, and 28-pad LCC packages. Commercial and industrial temperature devices are also available.

4

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

$A_0 - A_{12}$	Address Inputs
$\bar{W}$	Write Enable
$DQ_0 - DQ_7$	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{NE}$	Nonvolatile Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS}-0.6V to 7.0V
 Voltage on $DQ_0, 7$ and $\bar{G}$-0.5V to ($V_{CC}+0.5V$)
 Temperature under bias.....-55°C to 125°C
 Storage temperature.....-65°C to 150°C
 Power dissipation.....1W
 DC output current.....15mA

(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}^b	Average V_{CC} Current		90 85 80	mA	$t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ $t_{AVAV} = 55ns$
I_{CC2}^d	Average V_{CC} Current during STORE cycle		50	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		27 23 20	mA	$t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ $t_{AVAV} = 55ns$ $\bar{E} \geq V_{IH}$; all others cycling
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		2	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	-55	125	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: I_{CC2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels..... V_{SS} to 3V
 Input Rise and Fall Times..... $\leq 5ns$
 Input and Output Timing Reference Levels..... 1.5V
 Output Load..... See Figure 1

CAPACITANCE^e ($T_A=25^\circ C$, $f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

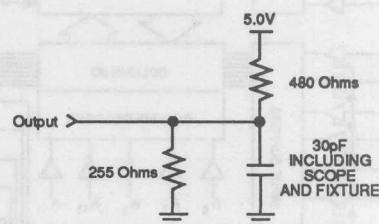


Figure 1: AC Output Loading

READ CYCLES #1 & #2
 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK10C68-35M		STK10C68-45M		STK10C68-55M		UNITS
	#1, #2	Alt		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELOV}	t_{ACS}	Chip Enable Access Time		35		45		55	ns
2	t_{AVAV}^g	t_{RC}	Read Cycle Time	35		45		55		ns
3	t_{AVOV}^h	t_{AA}	Address Access Time		35		45		55	ns
4	t_{GLOV}	t_{OE}	Output Enable to Data Valid		20		25		25	ns
5	t_{AXOX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELOX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHOZ}^i	t_{HZ}	Chip Disable to Output Inactive		17		20		25	ns
8	t_{GLOX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHOZ}^i	t_{OHZ}	Output Disable to Output Inactive		17		20		25	ns
10	t_{ELICCH}^e	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{c,e}$	t_{PS}	Chip Disable to Power Standby		35		45		55	ns
11A	t_{WHOV}	t_{WR}	Write Recovery Time		45		55		65	ns

Note c: Bringing $\bar{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

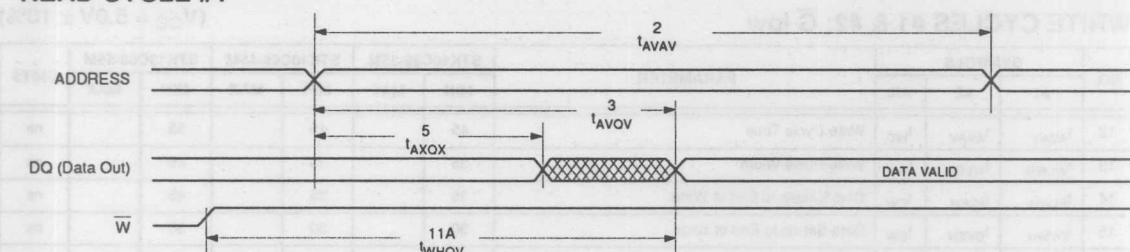
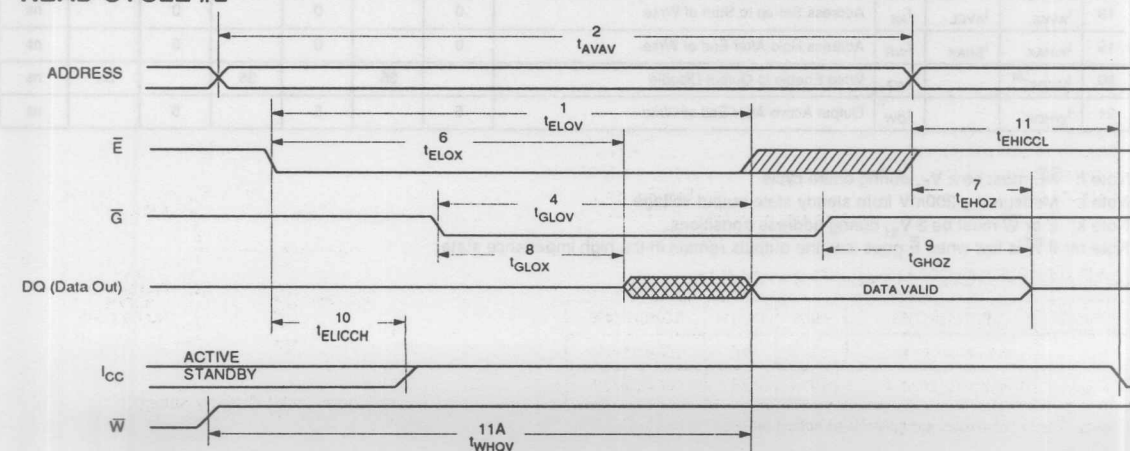
Note e: Parameter guaranteed but not tested.

Note f: $\bar{NE}$ must be high during entire cycle.

Note g: For READ CYCLE #1 and #2, $\bar{W}$ and $\bar{NE}$ must be high for entire cycle.

Note h: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note i: Measured $\pm 200mV$ from steady state output voltage.

READ CYCLE #1 f,g,h

READ CYCLE #2 f,g


STK10C68-M

WRITE CYCLES #1 & #2; $\overline{G}$ high

($V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOLS			PARAMETER	STK10C68-35M		STK10C68-45M		STK10C68-55M		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	35		45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	30		35		45		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	30		35		45		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	18		20		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	30		35		45		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns

WRITE CYCLES #1 & #2; $\overline{G}$ low

($V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOLS			PARAMETER	STK10C68-35M		STK10C68-45M		STK10C68-55M		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	45		45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	35		35		45		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	35		35		45		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	30		30		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	35		35		45		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	t_{WLOZ}^{im}		t_{WZ}	Write Enable to Output Disable		35		35		35	ns
21	t_{WHOX}		t_{OW}	Output Active After End of Write	5		5		5		ns

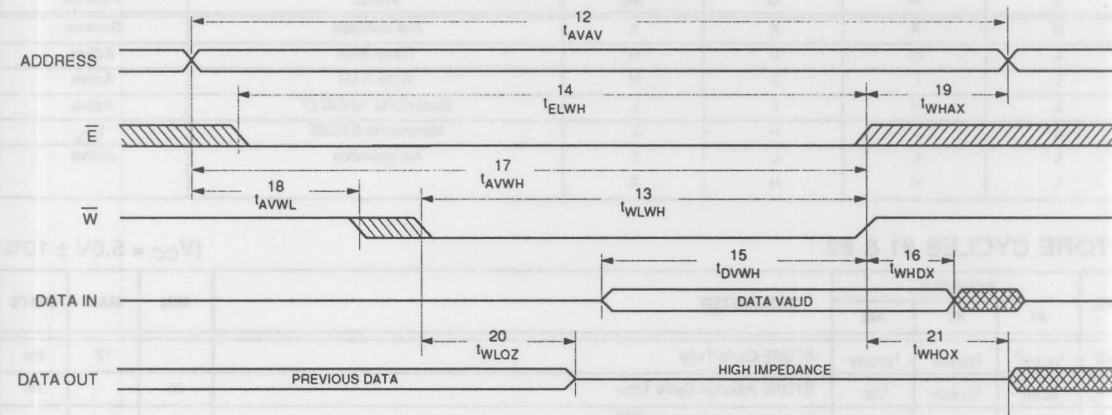
Note f: $\overline{NE}$ must be $\geq V_{IH}$ during entire cycle.

Note i: Measured $\pm 200mV$ from steady state output voltage.

Note k: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

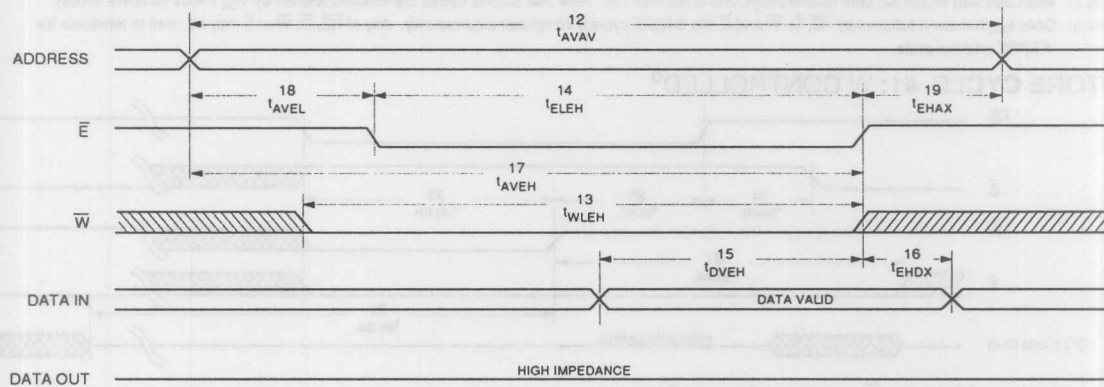
Note m: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: W CONTROLLED f, k



4

WRITE CYCLE #2: E CONTROLLED f, k



NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$	MODE	POWER
H	X	X	X	Not Selected	Standby
L	H	L	H	Read RAM	Active
L	L	X	H	Write RAM	Active
L	H	L	L	Nonvolatile <i>RECALL</i> ⁿ	Active
L	L	H	L	Nonvolatile <i>STORE</i>	I_{CC2}
L	L	L	L	No operation	Active
L	H	H	X		

STORE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

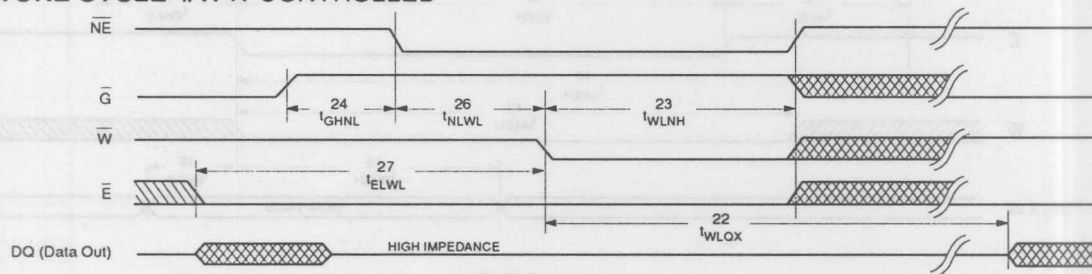
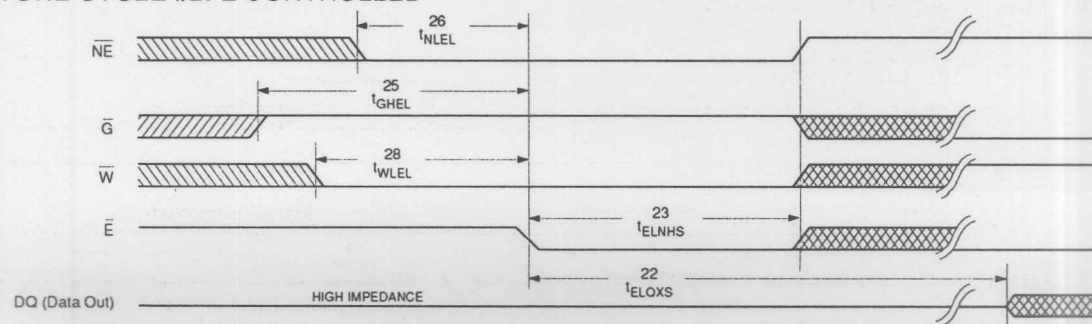
NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt.				
22	t_{WLOX}^p	t_{ELOXS}	t_{STORE}	STORE Cycle Time		12	ms
23	t_{WLNH}^q	t_{ELNHS}	t_{WC}	STORE Initiation Cycle Time	35		ns
24	t_{GHNL}			Output Disable Set-up to $\overline{NE}$ Fall	0		ns
25		t_{GHLE}		Output Disable Set-up to $\overline{E}$ Fall	0		ns
26	t_{NLWL}	t_{NLEL}		$\overline{NE}$ Set-up	0		ns
27	t_{ELWL}			Chip Enable Set-up	0		ns
28		t_{WLEL}		Write Enable Set-up	0		ns

Note n: An automatic *RECALL* also takes place at power up, starting when V_{CC} exceeds 4.0V, and taking t_{RECALL} from the time at which V_{CC} exceeds 4.5V. V_{CC} must not drop below 4.0V once it has been exceeded for the *RECALL* to function properly.

Note o: If $\overline{E}$ is low for any period of time in which $\overline{W}$ is high and $\overline{G}$ and $\overline{NE}$ are low, then a *RECALL* cycle may be initiated.

Note p: Measured with $\overline{W}$ and $\overline{NE}$ both returned high, and $\overline{G}$ returned low. Note that *STORE* cycles are inhibited/aborted by V_{CC} < 4.0V (*STORE* inhibit).

Note q: Once t_{WC} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the *STORE* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$, $\overline{W}$ or $\overline{E}$ may be used to terminate the *STORE* initiation cycle.

STORE CYCLE #1: $\overline{W}$ CONTROLLED^oSTORE CYCLE #2: $\overline{E}$ CONTROLLED^o

RECALL CYCLES #1, #2 & #3

(V_{CC} = 5.0V ± 10%)

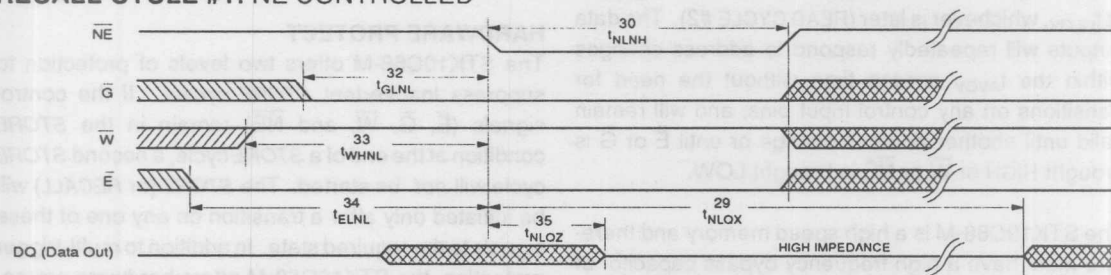
NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	#3				
29	t _{NLOX} ^r	t _{ELOXR}	t _{GLOXR}	RECALL Cycle Time		25	μs
30	t _{NLNH} ^s	t _{ELNHR}	t _{GLNH}	RECALL Initiation Cycle Time	35		ns
31		t _{NLEL}	t _{NLGL}	$\overline{NE}$ Set-up	0		ns
32	t _{GLNL}	t _{GLEL}		Output Enable Set-up	0		ns
33	t _{WHNL}	t _{WHEL}	t _{WHGL}	Write Enable Set-up	0		ns
34	t _{ELNL}		t _{ELGL}	Chip Enable Set-up	0		ns
35	t _{NLOZ}			$\overline{NE}$ Fall to Outputs Inactive		35	ns

Note r: Measured with $\overline{W}$ and $\overline{NE}$ both high, and $\overline{G}$ and $\overline{E}$ low.

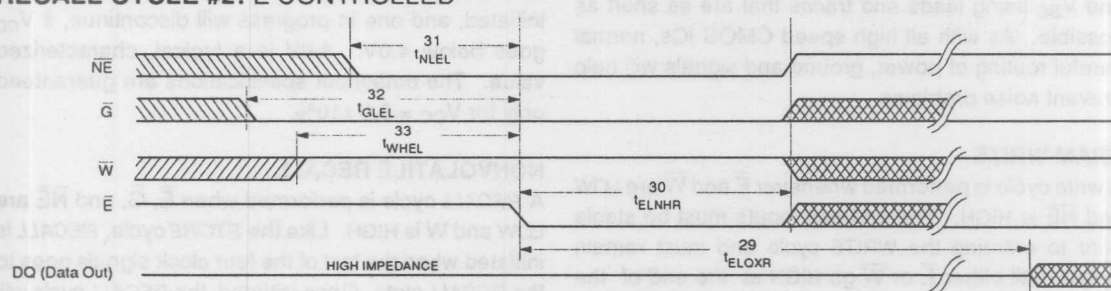
Note s: Once t_{NLNH} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the RECALL cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$ or $\overline{E}$ may be used to terminate the RECALL initiation cycle.

Note t: If $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ is high, then a STORE cycle will be initiated instead of a RECALL.

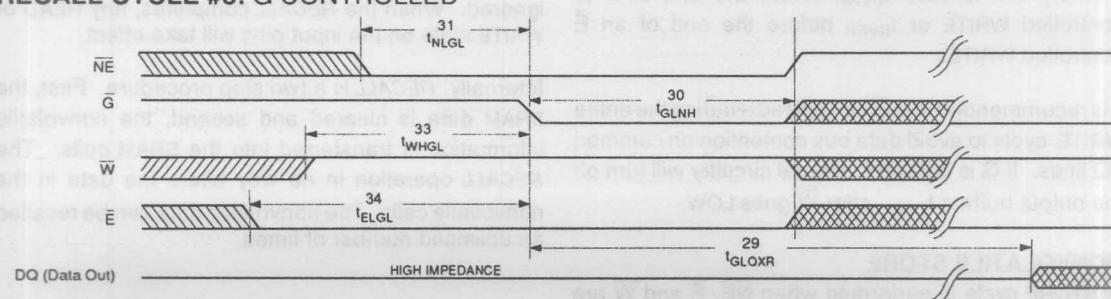
RECALL CYCLE #1: $\overline{NE}$ CONTROLLED^o



RECALL CYCLE #2: $\overline{E}$ CONTROLLED^o



RECALL CYCLE #3: $\overline{G}$ CONTROLLED^{o,t}



DEVICE OPERATION

The STK10C68-M has two modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pin. When in SRAM mode, the memory operates as a standard fast static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

SRAM READ

The STK10C68-M performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{NE}$ is brought LOW.

The STK10C68-M is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1 μF connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes LOW.

NONVOLATILE STORE

A STORE cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are

LOW and $\overline{G}$ is HIGH. While any sequence to achieve this state will initiate a STORE, only W initiation (STORE CYCLE #1) and $\overline{E}$ initiation (STORE CYCLE #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a STORE cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a STORE cycle is initiated, further input and output is disabled and the DQ_{0-7} pins are tri-stated until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the STORE.

HARDWARE PROTECT

The STK10C68-M offers two levels of protection to suppress inadvertent STORE cycles. If the control signals ($\overline{E}$, $\overline{G}$, $\overline{W}$, and $\overline{NE}$) remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will *not* be started. The STORE (or RECALL) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the STK10C68-M offers hardware protection through V_{CC} Sense. A STORE cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC} = 5.0 \pm 10\%$.

NONVOLATILE RECALL

A RECALL cycle is performed when $\overline{E}$, $\overline{G}$, and $\overline{NE}$ are LOW and W is HIGH. Like the STORE cycle, RECALL is initiated when the last of the four clock signals goes to the RECALL state. Once initiated, the RECALL cycle will take t_{NLQX} to complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pins will take effect.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the *STORE* cycle, a transition must occur on some control pin to cause a recall, preventing inadvertent multi-triggering. On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.0V once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic

RECALL, SRAM operation cannot commence until t_{NLQX} after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK10C68-M is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system V_{CC} .

ORDERING INFORMATION

STK10C68 - 5 C 35 M

Temperature Range

M = Military (-55 to 125 degrees C)

Access Time

35 = 35ns

45 = 45ns

55 = 55ns

Package

C = Ceramic 28 pin 300-mil DIP with gold lead finish

K = Ceramic 28 pin 300-mil DIP with solder DIP finish

L = Ceramic 28 pin LCC

Retention / Endurance

10 years / 100,000 cycles

5962-93056 04 MX X

Lead Finish

A = Solder DIP lead finish

C = Gold lead DIP finish

X = Lead finish "A" or "C" is acceptable

Package

MX = Ceramic 28 pin 300-mil DIP

MY = Ceramic 28 pin LCC

Access Time

04 = 55ns

05 = 45ns

06 = 35ns



STK11C68

CMOS nvSRAM

High Performance

8K x 8 Nonvolatile Static RAM

FEATURES

- 25, 30, 35 and 45ns Access Times
- 12, 15, 20 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Software *STORE* Initiation
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Software *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single 5V±10% Operation
- Commercial and Industrial Temperatures
- Available in multiple standard packages

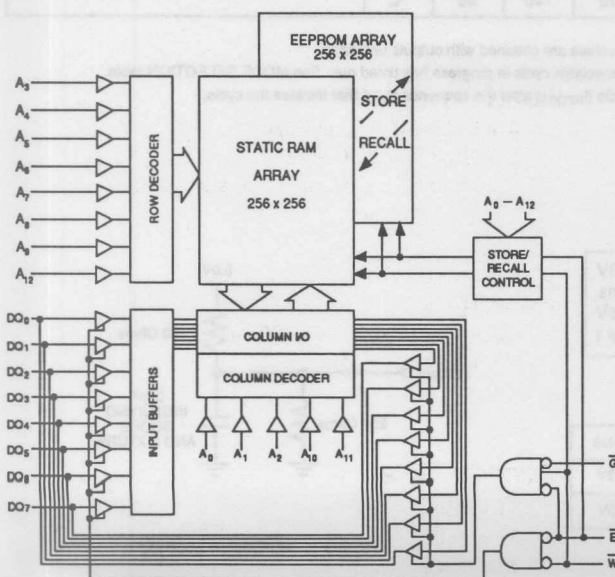
DESCRIPTION

The Simtek STK11C68 is a fast static RAM (25, 30, 35, 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) are initiated through software sequences. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

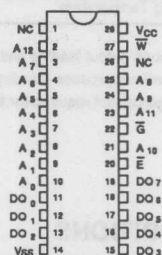
The STK11C68 is pin compatible with industry standard SRAMs and is available in a 28-pin 300 mil plastic or ceramic DIP, and a 28-pin SOIC. MIL-STD-883 and Standard Military Drawing (SMD 5962-92324) devices are also available.

4

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A ₀ - A ₁₂	Address Inputs
$\bar{W}$	Write Enable
DO ₀ - DO ₇	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS} -0.6V to 7.0V
 Voltage on $DQ_{0,7}$ and $\bar{Q}$ -0.5V to $(V_{CC}+0.5V)$
 Temperature under bias -55°C to 125°C
 Storage temperature -65°C to 150°C
 Power dissipation 1W
 DC output current 15mA
 (One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		90		95	mA	$t_{AVAV} = 25ns$
			85		90	mA	$t_{AVAV} = 30ns$
			80		85	mA	$t_{AVAV} = 35ns$
			75		80	mA	$t_{AVAV} = 45ns$
I_{CC2}^d	Average V_{CC} Current during STORE cycle		50		50	mA	$E \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30		34	mA	$t_{AVAV} = 25ns$
			27		30	mA	$t_{AVAV} = 30ns$
			23		27	mA	$t_{AVAV} = 35ns$
			20		23	mA	$t_{AVAV} = 45ns$
							$E \geq V_{IH}$; all others cycling
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		1		1	mA	$E \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{LK}	Input Leakage Current (Any Input)		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5		± 5	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage		2.4		2.4	V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $E \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: I_{CC2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels. V_{SS} to 3V
 Input Rise and Fall Times. $\leq 5ns$
 Input and Output Timing Reference Levels. 1.5V
 Output Load. See Figure 1

CAPACITANCE^e ($T_A=25^\circ C$, $f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

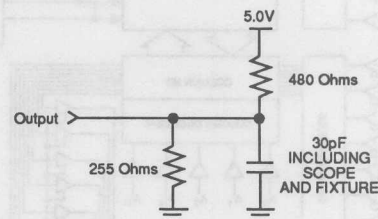


Figure 1: AC Output Loading

READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK11C68-25		STK11C68-30		STK11C68-35		STK11C68-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t _{ELOV}	t _{ACS}	Chip Enable Access Time		25		30		35		45	ns
2	t _{AVAV} ^g	t _{RC}	Read Cycle Time	25		30		35		45		ns
3	t _{AVQV} ^h	t _{AA}	Address Access Time		25		30		35		45	ns
4	t _{GLOV}	t _{OE}	Output Enable to Data Valid		12		15		20		25	ns
5	t _{AXOX}	t _{OH}	Output Hold After Address Change	5		5		5		5		ns
6	t _{ELOX}	t _{LZ}	Chip Enable to Output Active	5		5		5		5		ns
7	t _{EHQZ} ⁱ	t _{HZ}	Chip Disable to Output Inactive		13		15		17		20	ns
8	t _{GLOX}	t _{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t _{GHOZ} ⁱ	t _{OHZ}	Output Disable to Output Inactive		13		15		17		20	ns
10	t _{ELICCH} ^e	t _{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t _{EHICCL} ^{c,e}	t _{PS}	Chip Disable to Power Standby		25		30		35		45	ns
11A	t _{WHQV}	t _{WR}	Write Recovery Time		30		35		45		55	ns

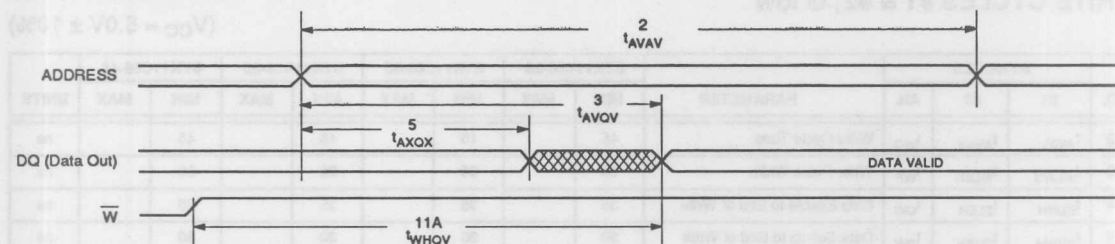
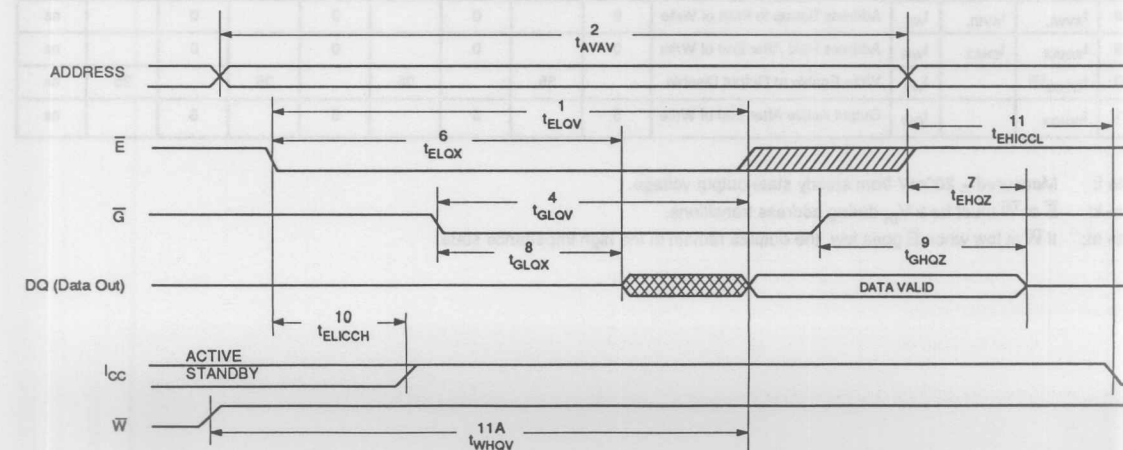
Note c: Bringing $\bar{E} \geq$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note e: Parameter guaranteed but not tested.

Note g: For READ CYCLE #1 and #2, $\bar{W}$ must be high for entire cycle.

Note h: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note i: Measured ± 200mV from steady state output voltage.

READ CYCLE #1^{g,h}READ CYCLE #2^g

WRITE CYCLES #1 & #2; $\overline{G}$ high $(V_{CC} = 5.0V \pm 10\%)$

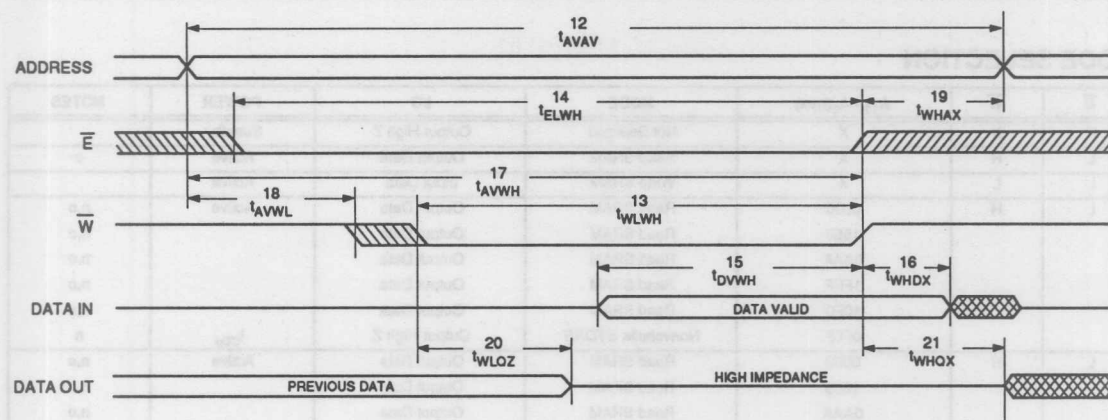
NO.	SYMBOLS			PARAMETER	STK11C68-25		STK11C68-30		STK11C68-35		STK11C68-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		30		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	12		15		18		20		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns

WRITE CYCLES #1 & #2; $\overline{G}$ low $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	STK11C68-25		STK11C68-30		STK11C68-35		STK11C68-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	45		45		45		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	35		35		35		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	35		35		35		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	30		30		30		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	35		35		35		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns
20	t_{WLOZ}^{Im}		t_{WZ}	Write Enable to Output Disable		35		35		35		35	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		5		ns

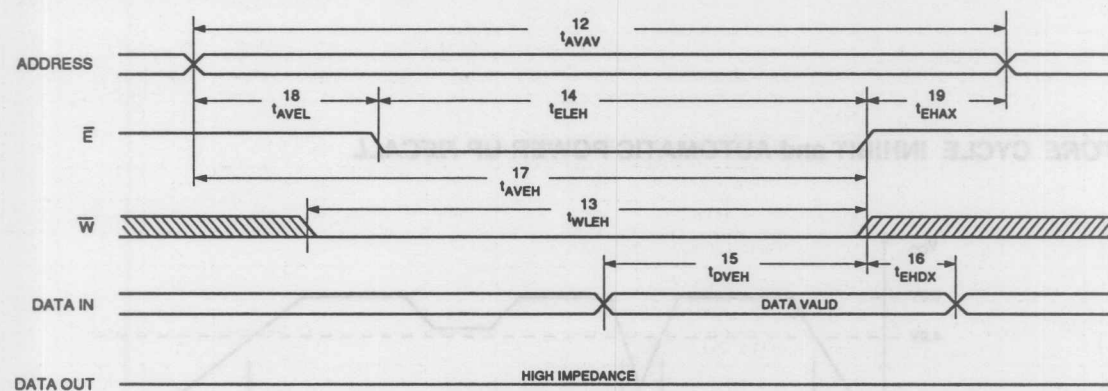
Note i: Measured $\pm 200mV$ from steady state output voltage.Note k: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.Note m: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\overline{W}$ CONTROLLED ^k



4

WRITE CYCLE #2: $\overline{E}$ CONTROLLED ^k



NONVOLATILE MEMORY OPERATION

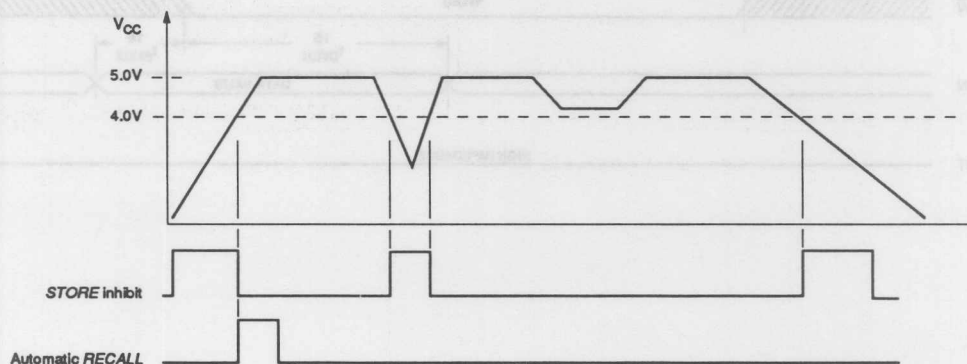
MODE SELECTION

$\overline{E}$	$\overline{W}$	$A_{12} - A_0(\text{hex})$	MODE	I/O	POWER	NOTES
H	X	X	Not Selected	Output High Z	Standby	
L	H	X	Read SRAM	Output Data	Active	o
L	L	X	Write SRAM	Input Data	Active	
L	H	0000	Read SRAM	Output Data	Active	n,o
		1555	Read SRAM	Output Data		n,o
		0AAA	Read SRAM	Output Data		n,o
		1FFF	Read SRAM	Output Data		n,o
		10F0	Read SRAM	Output Data		n,o
		0F0F	Nonvolatile <i>STORE</i>	Output High Z	I_{CC2}	n
L	H	0000	Read SRAM	Output Data	Active	n,o
		1555	Read SRAM	Output Data		n,o
		0AAA	Read SRAM	Output Data		n,o
		1FFF	Read SRAM	Output Data		n,o
		10F0	Read SRAM	Output Data		n,o
		0F0E	Nonvolatile <i>RECALL</i>	Output High Z		n

Note n: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a *STORE* cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles. See *STORE* cycle and *RECALL* cycle tables and diagrams for further details.

Note o: I/O state assumes that $\overline{G} \leq V_{IL}$. Initiation and operation of nonvolatile cycles does not depend on the state of $\overline{G}$.

STORE CYCLE INHIBIT and AUTOMATIC POWER-UP RECALL



STORE/RECALL CYCLE

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK11C68-25		STK11C68-30		STK11C68-35		STK11C68-45		UNITS
	#1	AIL		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
22	t _{AVAV}	t _{RC}	STORE/RECALL Initiation Cycle Time	25		30		35		45		ns
23	t _{ELOZ} ^p		Chip Enable to Output Inactive		75		75		75		75	ns
24	t _{ELOXS}	t _{STORE} ^q	STORE Cycle Time		10		10		10		10	ms
25	t _{ELOXR}	t _{RECALL} ^r	RECALL Cycle Time		20		20		20		20	μs
26	t _{AVELN} ^s	t _{AE}	Address Set-up to Chip Enable	0		0		0		0		ns
27	t _{ELEHN} ^{s,1}	t _{EP}	Chip Enable Pulse Width	15		20		25		35		ns
28	t _{EHAXN} ^s	t _{EA}	Chip Disable to Address Change	0		0		0		0		ns

Note p: Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.

Note q: Note that STORE cycles (but not RECALLs) are aborted by V_{CC} < 4.0V (STORE inhibit).

Note r: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds 4.0V. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

Note s: Noise on the $\bar{E}$ pin may trigger multiple read cycles from the same address and abort the address sequence.

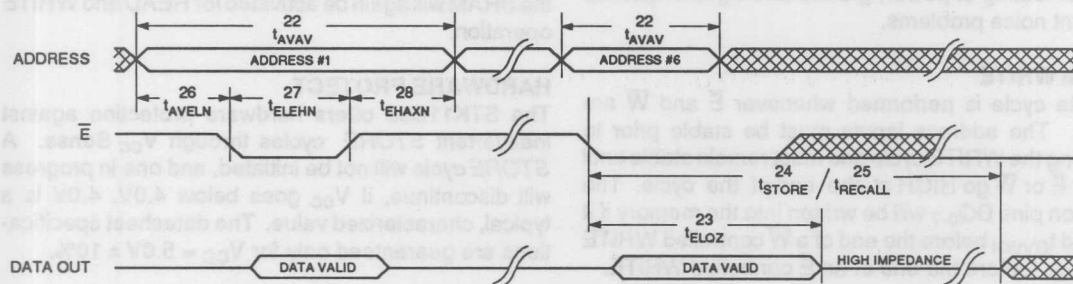
Note t: If the Chip Enable Pulse Width is less than t_{ELOV} (see READ CYCLE #2) but greater than or equal to t_{ELEHN}, then the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.

Note u: $\bar{W}$ must be HIGH when $\bar{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\bar{G}$ may be either HIGH or LOW throughout.

Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK11C68 performs a STORE or RECALL.

Note v: $\bar{E}$ must be used to clock in the address sequence for the Software STORE and RECALL cycles.

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STORE/RECALL CYCLE^{u,v}

DEVICE OPERATION

The STK11C68 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile operation, data is transferred from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

SRAM READ

The STK11C68 performs a READ cycle whenever $\bar{E}$ and $\bar{G}$ are LOW while $\bar{W}$ is HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\bar{E}$ or $\bar{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\bar{E}$ or $\bar{G}$ is brought HIGH or $\bar{W}$ is brought LOW.

The STK11C68 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately $0.1\mu F$ connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\bar{E}$ and $\bar{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\bar{E}$ or $\bar{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\bar{W}$ controlled WRITE or t_{DVEH} before the end of an $\bar{E}$ controlled WRITE.

It is recommended that $\bar{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\bar{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\bar{W}$ goes LOW.

NONVOLATILE STORE

The STK11C68 *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the STK11C68 implements nonvolatile operation while remaining pin-for-pin compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the

previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for *STORE* initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the *STORE* cycle the following READ sequence must be performed:

1. Read address	0000 (hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0F (hex)	Initiate <i>STORE</i> Cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\bar{G}$ be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

HARDWARE PROTECT

The STK11C68 offers hardware protection against inadvertent *STORE* cycles through V_{CC} Sense. A *STORE* cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC} = 5.0V \pm 10\%$.

NONVOLATILE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

1. Read address	0000 (hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0E (hex)	Initiate <i>RECALL</i> Cycle

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

On power-up, once V_{CC} exceeds the V_{CC} Sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.0V

once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{RECALL} after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK11C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system V_{CC} .

ORDERING INFORMATION

STK11C68 - P 35 I

Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

25 = 25ns

30 = 30ns

35 = 35ns

45 = 45ns

Package

P = Plastic 28 pin 300 mil DIP

C = Ceramic 28 pin 300 mil DIP

S = Plastic 28 pin SOIC



STK11C68-M

CMOS nvSRAM

High Performance

8K x 8 Nonvolatile Static RAM

MIL-STD-883/SMD # 5962-92324

FEATURES

- 35, 45 and 55ns Access Times
- 25 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Software *STORE* Initiation
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Software *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single 5V $\pm 10\%$ Operation
- Available in multiple standard packages

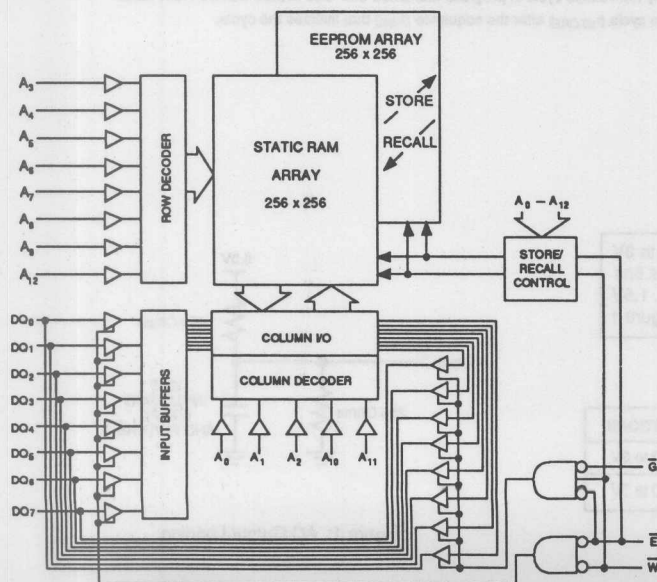
DESCRIPTION

The Simtek STK11C68-M is a fast static RAM (35, 45 and 55ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) are initiated through software sequences. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

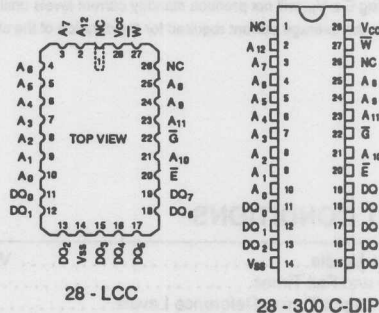
The STK11C68-M is pin compatible with industry standard SRAMs and is available in a 28-pin 300 mil ceramic DIP or 28-pad LCC package. Commercial and industrial devices are also available.

4

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A ₀ - A ₁₂	Address Inputs
W	Write Enable
DQ ₀ - DQ ₇	Data In/Out
E	Chip Enable
G	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS} -0.6V to 7.0V
 Voltage on DQ₀₋₇ and $\bar{Q}$ -0.5V to ($V_{CC}+0.5V$)
 Temperature under bias -55°C to 125°C
 Storage temperature -65°C to 150°C
 Power dissipation 1W
 DC output current 15mA
 (One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}^b	Average V_{CC} Current		90 85 80	mA mA mA	$t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ $t_{AVAV} = 55ns$
I_{CC2}^d	Average V_{CC} Current during STORE cycle		50	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		27 23 20	mA mA mA	$t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ $t_{AVAV} = 55ns$ $\bar{E} \geq V_{IH}$; all others cycling
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		2	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	-55	125	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: I_{CC2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels V_{SS} to 3V
 Input Rise and Fall Times $\leq 5ns$
 Input and Output Timing Reference Levels 1.5V
 Output Load See Figure 1

CAPACITANCE^e ($T_A=25^\circ C$, $f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

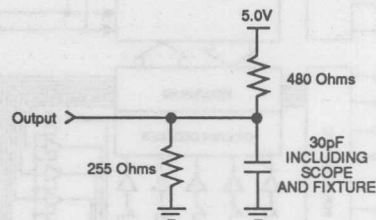


Figure 1: AC Output Loading

READ CYCLES #1 & #2

($V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOLS		PARAMETER	STK11C68-35M		STK11C68-45M		STK11C68-55M		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}^g	t_{ACS}	Chip Enable Access Time		35		45		55	ns
2	t_{AVAV}^g	t_{RC}	Read Cycle Time	35		45		55		ns
3	t_{AVQV}^h	t_{AA}	Address Access Time		35		45		55	ns
4	t_{GLOV}	t_{OE}	Output Enable to Data Valid		20		25		25	ns
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELOX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}^i	t_{HZ}	Chip Disable to Output Inactive		17		20		25	ns
8	t_{GLOX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}^i	t_{OHZ}	Output Disable to Output Inactive		17		20		25	ns
10	t_{ELICCH}^e	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{e,g}$	t_{PS}	Chip Disable to Power Standby		35		45		55	ns
11A	t_{WHQV}	t_{WR}	Write Recovery Time		45		55		65	ns

Note c: Bringing $\bar{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

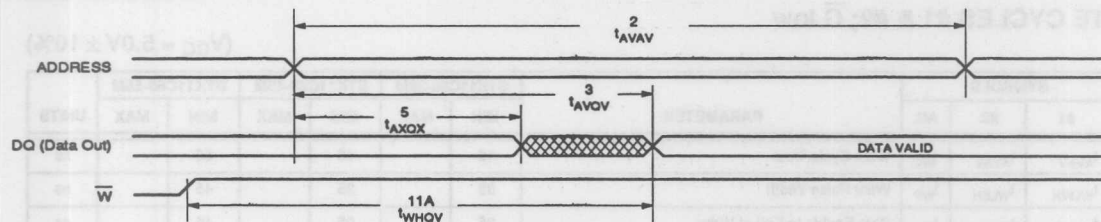
Note e: Parameter guaranteed but not tested.

Note g: For READ CYCLE #1 and #2, $\bar{W}$ must be high for entire cycle.

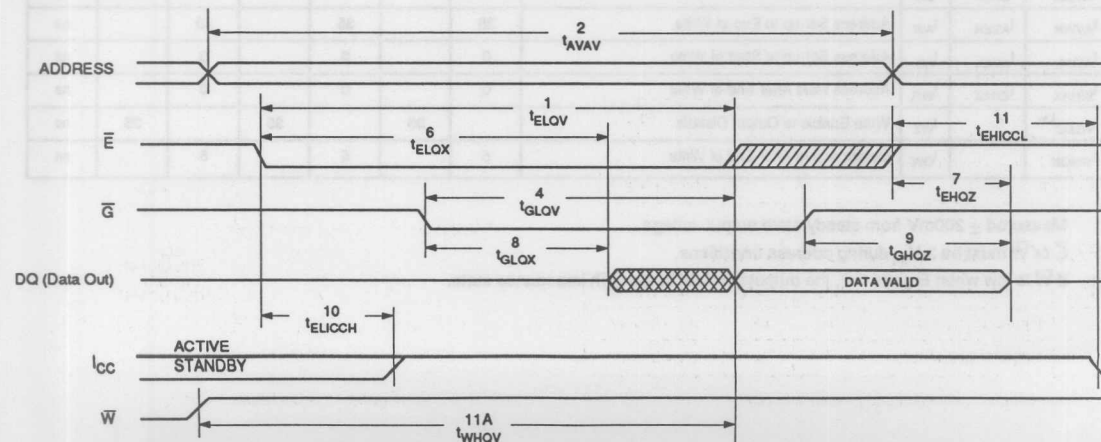
Note h: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note i: Measured $\pm 200mV$ from steady state output voltage.

READ CYCLE #1 ^{g,h}



READ CYCLE #2 ^g



WRITE CYCLES #1 & #2; $\bar{G}$ high(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	STK11C68-35M		STK11C68-45M		STK11C68-55M		UNITS
	#1	#2	Alt		MIN	MAX	MIN	MAX	MIN	MAX	
12	t _{AVAV}	t _{AVAV}	t _{WC}	Write Cycle Time	35		45		55		ns
13	t _{WLWH}	t _{WLEH}	t _{WP}	Write Pulse Width	30		35		45		ns
14	t _{ELWH}	t _{ELEH}	t _{CW}	Chip Enable to End of Write	30		35		45		ns
15	t _{DVWH}	t _{DVEH}	t _{DW}	Data Set-up to End of Write	18		20		30		ns
16	t _{WHDX}	t _{EHDx}	t _{DH}	Data Hold After End of Write	0		0		0		ns
17	t _{AVWH}	t _{AVEH}	t _{AW}	Address Set-up to End of Write	30		35		45		ns
18	t _{AVWL}	t _{AVEL}	t _{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t _{WHAX}	t _{EHAX}	t _{WR}	Address Hold After End of Write	0		0		0		ns

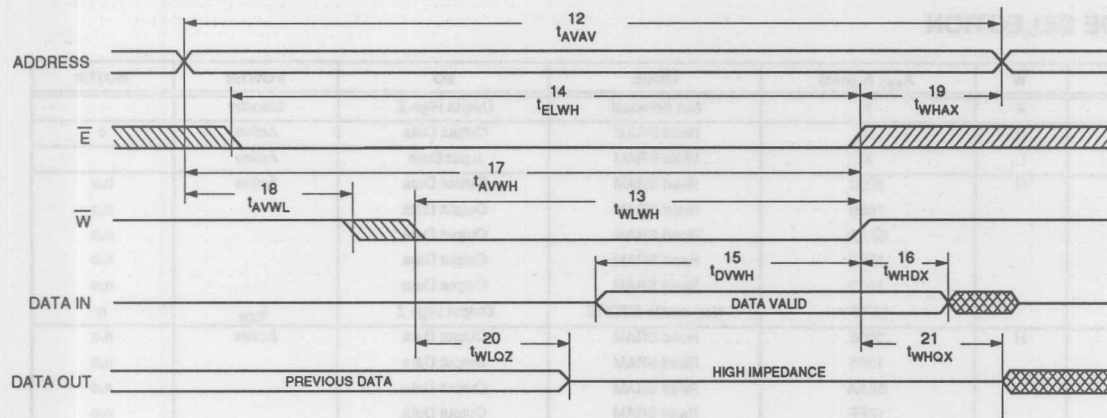
WRITE CYCLES #1 & #2; $\bar{G}$ low(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	STK11C68-35M		STK11C68-45M		STK11C68-55M		UNITS
	#1	#2	Alt		MIN	MAX	MIN	MAX	MIN	MAX	
12	t _{AVAV}	t _{AVAV}	t _{WC}	Write Cycle Time	45		45		55		ns
13	t _{WLWH}	t _{WLEH}	t _{WP}	Write Pulse Width	35		35		45		ns
14	t _{ELWH}	t _{ELEH}	t _{CW}	Chip Enable to End of Write	35		35		45		ns
15	t _{DVWH}	t _{DVEH}	t _{DW}	Data Set-up to End of Write	30		30		30		ns
16	t _{WHDX}	t _{EHDx}	t _{DH}	Data Hold After End of Write	0		0		0		ns
17	t _{AVWH}	t _{AVEH}	t _{AW}	Address Set-up to End of Write	35		35		45		ns
18	t _{AVWL}	t _{AVEL}	t _{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t _{WHAX}	t _{EHAX}	t _{WR}	Address Hold After End of Write	0		0		0		ns
20	t _{WLOZ} ^{1m}		t _{WZ}	Write Enable to Output Disable		35		35		35	ns
21	t _{WHOX}		t _{OW}	Output Active After End of Write	5		5		5		ns

Note i: Measured ± 200mV from steady state output voltage.

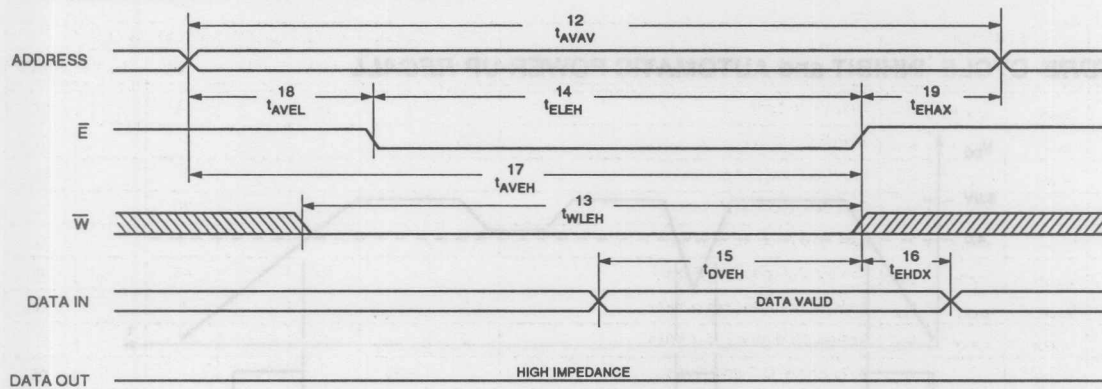
Note k: $\bar{E}$ or $\bar{W}$ must be ≥ V_{IH} during address transitions.Note m: If $\bar{W}$ is low when $\bar{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\overline{W}$ CONTROLLED^k



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WRITE CYCLE #2: $\overline{E}$ CONTROLLED^k



NONVOLATILE MEMORY OPERATION

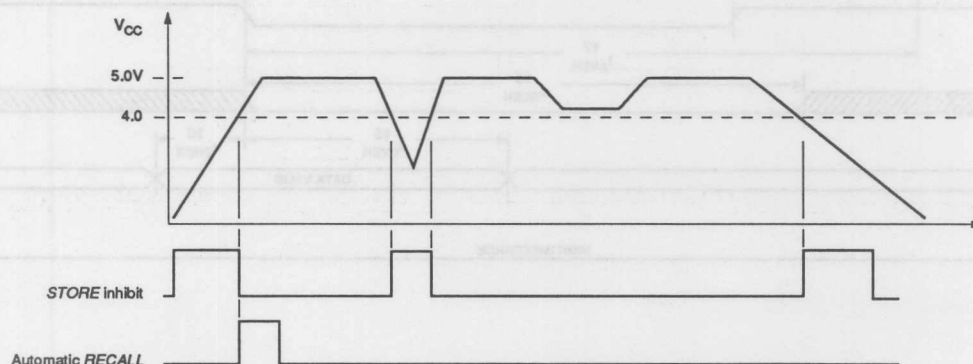
MODE SELECTION

$\bar{E}$	$\bar{W}$	$A_{12} - A_0(\text{hex})$	MODE	I/O	POWER	NOTES
H	X	X	Not Selected	Output High Z	Standby	
L	H	X	Read SRAM	Output Data	Active	o
L	L	X	Write SRAM	Input Data	Active	
L	H	0000	Read SRAM	Output Data	Active	n,o
		1555	Read SRAM	Output Data		n,o
		0AAA	Read SRAM	Output Data		n,o
		1FFF	Read SRAM	Output Data		n,o
		10F0	Read SRAM	Output Data		n,o
		0F0F	Nonvolatile <i>STORE</i>	Output High Z		n
L	H	0000	Read SRAM	Output Data	Active	n,o
		1555	Read SRAM	Output Data		n,o
		0AAA	Read SRAM	Output Data		n,o
		1FFF	Read SRAM	Output Data		n,o
		10F0	Read SRAM	Output Data		n,o
		0F0E	Nonvolatile <i>RECALL</i>	Output High Z		n

Note n: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a *STORE* cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a *RECALL* cycle. $\bar{W}$ must be high during all six consecutive cycles. See *STORE* cycle and *RECALL* cycle tables and diagrams for further details.

Note o: I/O state assumes that $\bar{G} \leq V_{IL}$. Initiation and operation of nonvolatile cycles does not depend on the state of $\bar{G}$.

STORE CYCLE INHIBIT and AUTOMATIC POWER-UP RECALL



STORE/RECALL CYCLE

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK11C68-35M		STK11C68-45M		STK11C68-55M		UNITS
	#1	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
22	t _{AVAV}	t _{RC}	STORE/RECALL Initiation Cycle Time	35		45		55		ns
23	t _{ELOZ} ^p		Chip Enable to Output Inactive		75		75		85	ns
24	t _{ELOXS}	t _{STORE} ^q	STORE Cycle Time		12		12		12	ms
25	t _{ELOXR}	t _{RECALL} ^r	RECALL Cycle Time		25		25		25	μs
26	t _{AVELN} ^s	t _{AE}	Address Set-up to Chip Enable	0		0		0		ns
27	t _{ELEHN} ^{s,t}	t _{EP}	Chip Enable Pulse Width	25		35		45		ns
28	t _{EHAXN} ^s	t _{EA}	Chip Disable to Address Change	0		0		0		ns

Note p: Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.

Note q: Note that STORE cycles (but not RECALLs) are aborted by V_{CC} < 4.0V (STORE Inhibit).

Note r: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds 4.0V. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

Note s: Noise on the $\bar{E}$ pin may trigger multiple read cycles from the same address and abort the address sequence.

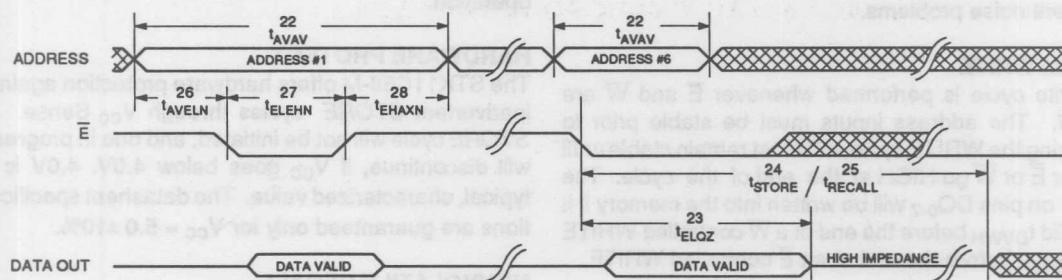
Note t: If the Chip Enable Pulse Width is less than t_{ELOV} (see READ CYCLE #2) but greater than or equal to t_{ELEHN}, then the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.

Note u: $\bar{W}$ must be HIGH when $\bar{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\bar{G}$ may be either HIGH or LOW throughout.

Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK11C68-M performs a STORE or RECALL.

Note v: $\bar{E}$ must be used to clock in the address sequence for the Software STORE and RECALL cycles.

4

STORE/RECALL CYCLE ^{u,v}

DEVICE OPERATION

The STK11C68-M has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

SRAM READ

The STK11C68-M performs a READ cycle whenever $\bar{E}$ and $\bar{G}$ are LOW while $\bar{W}$ is HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\bar{E}$ or $\bar{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\bar{E}$ or $\bar{G}$ is brought HIGH or $\bar{W}$ is brought LOW.

The STK11C68-M is a high speed memory and therefore must have a high frequency bypass capacitor of approximately $0.1\mu F$ connected between DUT V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM WRITE

A write cycle is performed whenever $\bar{E}$ and $\bar{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\bar{E}$ or $\bar{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\bar{W}$ controlled WRITE or t_{DVEH} before the end of an $\bar{E}$ controlled WRITE.

It is recommended that $\bar{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\bar{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\bar{W}$ goes LOW.

NONVOLATILE STORE

The STK11C68-M *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the STK11C68-M implements nonvolatile operation while remaining pin-for-pin compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the

previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for *STORE* initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the *STORE* cycle the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate <i>STORE</i> Cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\bar{G}$ be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

HARDWARE PROTECT

The STK11C68-M offers hardware protection against inadvertent *STORE* cycles through V_{CC} Sense. A *STORE* cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC} = 5.0 \pm 10\%$.

NONVOLATILE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate <i>RECALL</i> Cycle

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.0V

once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{RECALL} after V_{CC} exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK11C68-M is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system V_{CC} .

ORDERING INFORMATION

STK11C68 - 5 C 35 M

Temperature Range

M = Military (-55 to 125 degrees C)

Access Time

35 = 35ns

45 = 45ns

55 = 55ns

Package

C = Ceramic 28 pin 300-mil DIP with gold lead finish

K = Ceramic 28 pin 300-mil DIP with solder DIP finish

L = Ceramic 28 pin LCC

Retention / Endurance

10 years / 100,000 cycles

5962-92324 04 MX X

Lead Finish

A = Solder DIP lead finish

C = Gold lead DIP finish

X = lead finish "A" or "C" is acceptable

Package

MX = Ceramic 28 pin 300-mil DIP

MY = Ceramic 28 pin LCC

Access Time

04 = 55ns

05 = 45ns

06 = 35ns



STK12C68

CMOS nvSRAM

8K x 8 High Performance

AutoStore™ Nonvolatile Static RAM

FEATURES

- 30, 35 and 45ns Access Times
- 15 mA I_{CC} at 200ns Access Speed
- Automatic *STORE* to EEPROM on Power Down
- Hardware or Software Initiated *STORE* to EEPROM
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Software Initiated *RECALL* from EEPROM
- Unlimited *RECALL* cycles from EEPROM
- Single $5V \pm 10\%$ Operation
- Commercial and Industrial Temperatures
- Available in multiple standard packages

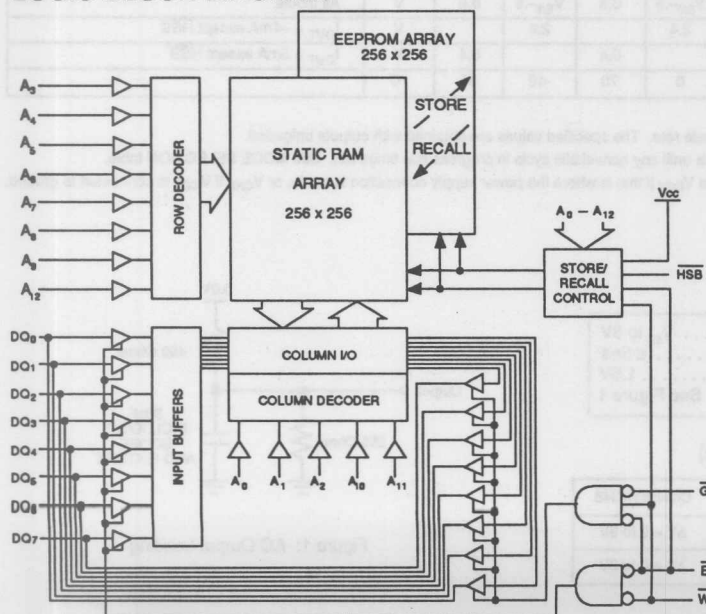
DESCRIPTION

The Simtek STK12C68 is a fast static RAM (30, 35 and 45ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) take place automatically upon power down using charge stored in an external 100 μ F capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on power up. Software sequences may also be used to initiate both *STORE* and *RECALL* operations. A *STORE* can also be initiated via a single pin.

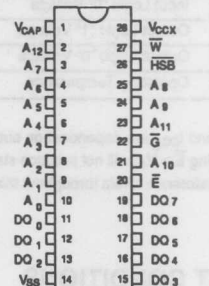
The STK12C68 is available in the following packages: a 28-pin 300 mil plastic or ceramic DIP, a 28-pin 600 mil plastic DIP and a 28-pin SOIC. MIL-STD-883 and Standard Military Drawing (SMD 5962-94599) devices are also available.

4

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 600 PDIP 28 - 350 SOIC
28 - 300 PDIP 28 - 300 CDIP

PIN NAMES

A ₀ - A ₁₂	Address Inputs
W	Write Enable
DQ ₀ - DQ ₇	Data In/Out
E	Chip Enable
G	Output Enable
V _{CCX}	Power (+5V)
V _{SS}	Ground
V _{CAP}	Capacitor
HSB	Hardware Store/Busy

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS} -0.6V to 7.0V
 Voltage on DQ₀₋₇ and $\bar{G}$ -0.5V to ($V_{CC}+0.5V$)
 Temperature under bias -55°C to 125°C
 Storage temperature -65°C to 150°C
 Power dissipation 1W
 DC output current 15mA
 (One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)^d

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average V_{CC} Current		85		95	mA	$t_{AVAV} = 30ns$
			80		85	mA	$t_{AVAV} = 35ns$
			75		80	mA	$t_{AVAV} = 45ns$
I_{CC2}	Average V_{CC} Current During STORE		6		7	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC3}^b	Average V_{CC} Current at $t_{AVAV} = 200ns$		15		15	mA	$\bar{E} \leq 0.2V, W \geq (V_{CC} - 0.2V)$ others $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	Average V_{CC} current during AutoStore™ Cycle		4		4	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		35		39	mA	$t_{AVAV} = 30ns$
			32		35	mA	$t_{AVAV} = 35ns$
			28		32	mA	$t_{AVAV} = 45ns$
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\bar{E} \geq V_{IH}$; all others cycling
							$\bar{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK3}	Input Leakage Current (Any Input)		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5		± 5	μA	$V_{CC} = \max$ $V_{OUT} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-0.5$	0.8	$V_{SS}-0.5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$ except HSB
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$ except HSB
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: V_{CC} reference levels throughout this datasheet refer to V_{CCX} if that is where the power supply connection is made, or V_{CAP} if V_{CCX} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels V_{SS} to 3V
 Input Rise and Fall Times $\leq 5ns$
 Input and Output Timing Reference Levels 1.5V
 Output Load See Figure 1

CAPACITANCE^e ($T_A = 25^\circ C, f = 1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

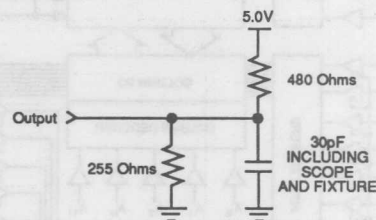


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

READ CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)^d$

NO.	SYMBOLS		PARAMETER	STK12C68-30		STK12C68-35		STK12C68-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELOV}	t_{ACS}	Chip Enable Access Time		30		35		45	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	30		35		45		ns
3	t_{AVOV}^g	t_{AA}	Address Access Time		30		35		45	ns
4	t_{GLOV}	t_{OE}	Output Enable to Data Valid		15		20		25	ns
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELOX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHOZ}^h	t_{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t_{GLOX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHOZ}^h	t_{OHZ}	Output Disable to Output Inactive		15		17		20	ns
10	t_{ELICCH}^e	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{c,e}$	t_{PS}	Chip Disable to Power Standby		30		35		45	ns

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

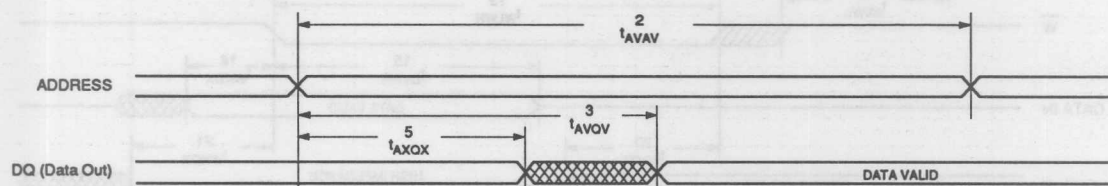
Note e: Parameter guaranteed but not tested.

Note f: For READ CYCLE #1 and #2, $\bar{W}$ is high for entire cycle.

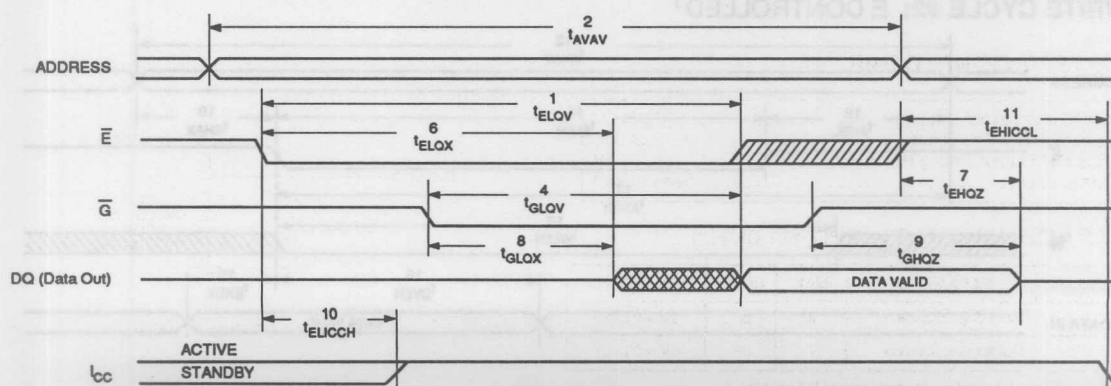
Note g: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note h: Measured $\pm 200mV$ from steady state output voltage.

READ CYCLE #1 ^{f,g}



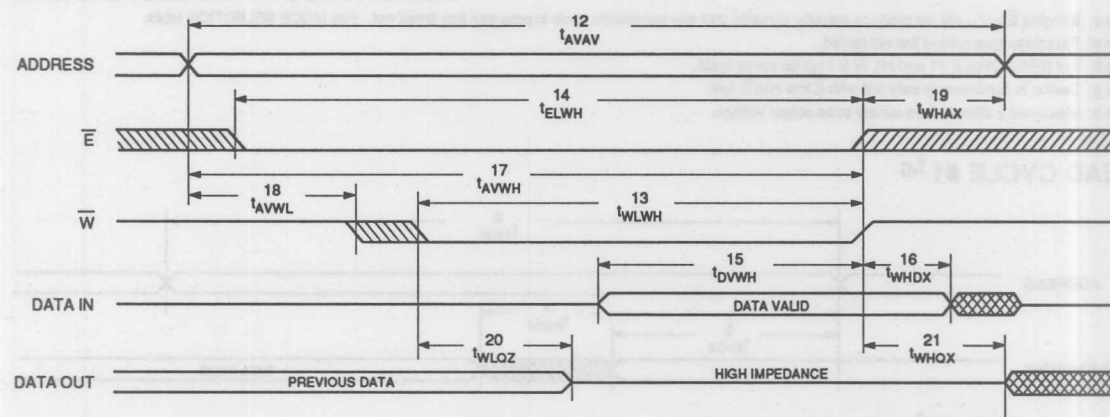
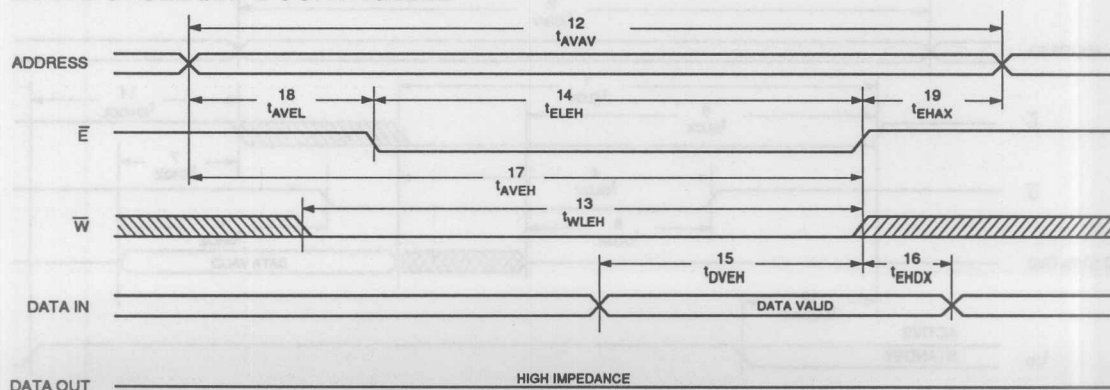
READ CYCLE #2 ^f



WRITE CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)^d$

NO.	SYMBOLS			PARAMETER	STK12C68-30		STK12C68-35		STK12C68-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	30		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	25		30		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	25		30		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		18		20		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	25		30		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	$t_{WLOZ}^{h,j}$		t_{WZ}	Write Enable to Output Disable		15		17		20	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note h: Measured $\pm 200mV$ from steady state output voltage.Note i: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ during address transitions.Note j: If $\bar{W}$ is low when $\bar{E}$ goes low, the outputs remain in the high impedance state.WRITE CYCLE #1: $\bar{W}$ CONTROLLEDⁱWRITE CYCLE #2: $\bar{E}$ CONTROLLEDⁱ

NONVOLATILE MEMORY OPERATION

MODE SELECTION

E	W	HSB	A ₁₂ - A ₀ (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	I
L	L	H	X	Write SRAM	Input Data	Active	
L	H	H	0000	Read SRAM	Output Data	Active	k,l
			1555	Read SRAM	Output Data		k,l
			0AAA	Read SRAM	Output Data		k,l
			1FFF	Read SRAM	Output Data		k,l
			10F0	Read SRAM	Output Data		k,l
			0F0F	Nonvolatile STORE	Output High Z		k
L	H	H	0000	Read SRAM	Output Data	Active	k,l
			1555	Read SRAM	Output Data		k,l
			0AAA	Read SRAM	Output Data		k,l
			1FFF	Read SRAM	Output Data		k,l
			10F0	Read SRAM	Output Data		k,l
			0F0E	Nonvolatile RECALL	Output High Z		k
X	X	L	X	STORE/Inhibit	Output High Z	I _{CC2} /Standby	m

Note k: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. W must be high during all six consecutive cycles. See STORE cycle and RECALL cycle tables and diagrams for further details.

Note l: I/O state assumes that $\bar{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on the state of $\bar{G}$.

Note m: HSB initiated STORE operation actually occurs only if a WRITE has been done since last STORE operation. After the STORE (if any) completes, the part will go into standby mode inhibiting all operation until HSB rises.

HARDWARE STORE/RECALL

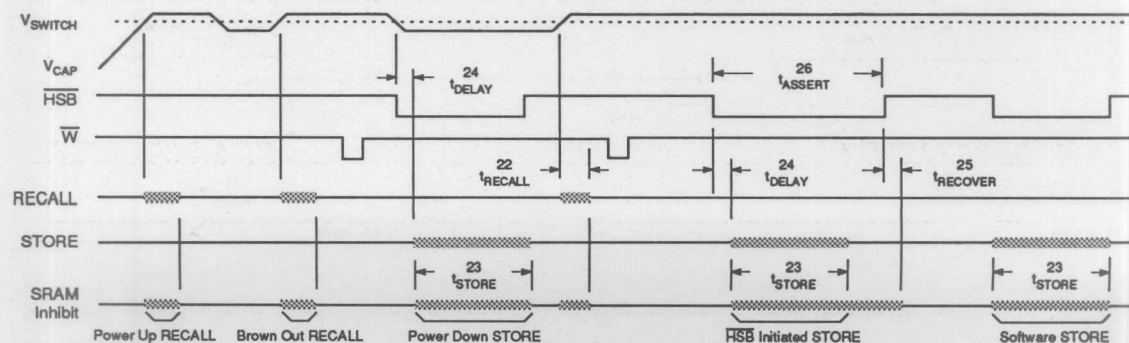
NO.	SYMBOLS	PARAMETER	MIN	MAX	UNITS	NOTES
22	t _{RECALL}	RECALL Cycle Duration		20	μs	Note o
23	t _{STORE}	STORE Cycle Duration		10	ms	V _{CC} ≥ 4.5V
24	t _{DELAY}	HSB Low to Inhibit On	1		μs	
25	t _{RECOVER}	HSB High to Inhibit Off		300	ns	Note e
26	t _{ASSERT}	External STORE Pulse Width	250		ns	Note e
	V _{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
	I _{HSB_OL}	HSB Output Low Current	3		mA	HSB = V _{OL} , Note e, n
	I _{HSB_OH}	HSB Output High Current	5	60	μA	HSB = V _{IL} , Note e, n

Note e: These parameters guaranteed but not tested.

Note n: HSB is an I/O that has a weak internal pullup; it is basically an open drain output. It is meant to allow up to 32 STK12C68s to be ganged together for simultaneous storing. Do not use HSB to pullup any external circuitry other than other STK12C68 HSB pins.

Note o: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds V_{SWITCH}. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

HARDWARE STORE/RECALL



SOFTWARE STORE/RECALL CYCLE

 $(V_{CC} = 5.0V \pm 10\%)^d$

NO.	SYMBOLS		PARAMETER	STK12C68-30		STK12C68-35		STK12C68-45		UNITS
	Std.	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
27	t_{AVAV}	t_{RC}	Store/Recall Initiation Cycle Time	30		35		45		ns
28	t_{ELOZ}^p		Chip Enable to Output Inactive		85		85		85	ns
29	t_{AVELN}	t_{AE}	Address Set-up to Chip Enable	0		0		0		ns
30	$t_{ELEHN}^{p,q}$	t_{EP}	Chip Enable Pulse Width	20		25		35		ns
31	t_{EHAXN}	t_{EA}	Chip Disable to Address Change	0		0		0		ns

Note p: Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.

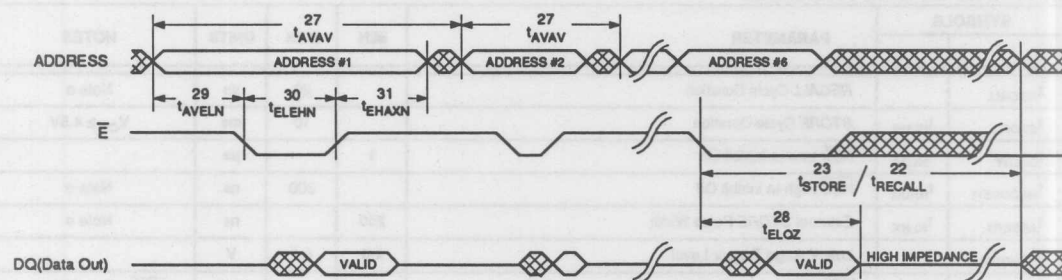
Note q: Noise on the $\bar{E}$ pin may trigger multiple read cycles from the same address and abort the address sequence.

Note r: If the Chip Enable Pulse Width is less than t_{ELOV} (see READ CYCLE #2) but greater than or equal to t_{ELEHN} , then the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.

Note s: $\bar{W}$ must be HIGH when $\bar{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\bar{G}$ may be either HIGH or LOW throughout.

Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK12C68 performs a STORE or RECALL.

Note t: $\bar{E}$ must be used to clock in the address sequence for the Software STORE and RECALL cycles.

SOFTWARE STORE/RECALL CYCLE ^{q,r,t}

DEVICE OPERATION

The STK12C68 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via a software sequence or $\overline{\text{HSB}}$ assertion and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH} . *RECALL* operations are automatically initiated upon power-up and whenever the power supply voltage level rises above V_{SWITCH} . *RECALL* cycles may also be initiated by a software sequence.

SRAM READ

The STK12C68 performs a READ cycle whenever $\overline{\text{E}}$ and $\overline{\text{G}}$ are LOW and $\overline{\text{HSB}}$ and $\overline{\text{W}}$ are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} . If the READ is initiated by $\overline{\text{E}}$ or $\overline{\text{G}}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later. The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{\text{E}}$ or $\overline{\text{G}}$ is brought HIGH or $\overline{\text{W}}$ or $\overline{\text{HSB}}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{\text{E}}$ and $\overline{\text{W}}$ are LOW and $\overline{\text{HSB}}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{\text{E}}$ or $\overline{\text{W}}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{\text{W}}$ controlled WRITE or t_{DVEH} before the end of an $\overline{\text{E}}$ controlled WRITE.

It is recommended that $\overline{\text{G}}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{\text{G}}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{\text{W}}$ goes LOW.

SOFTWARE STORE

The STK12C68 software *STORE* cycle is initiated by executing sequential READ cycles from six specific

address locations. By relying on READ cycles only, the STK12C68 implements nonvolatile operation while remaining compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into the nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of addresses is used for *STORE* initiation, it is critical that no other read or write accesses intervene in the sequence or the sequence will be aborted.

To initiate the *STORE* cycle the following READ sequence must be performed:

1. Read address	0000 (hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0F (hex)	Initiate <i>STORE</i> Cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{\text{G}}$ be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

1. Read address	0000(hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0E (hex)	Initiate <i>RECALL</i> Cycle

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the

EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AUTOMATIC RECALL

During power up, or after any low power condition ($V_{CAP} < V_{SWITCH}$), when V_{CAP} exceeds the sense voltage of V_{SWITCH} , a *RECALL* cycle will automatically be initiated. After the initiation of this automatic *RECALL*, if V_{CAP} falls below V_{SWITCH} , then another *RECALL* operation will be performed whenever V_{CAP} again rises above V_{SWITCH} .

If the STK12C68 is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between W and system V_{CC} .

HARDWARE PROTECT

The STK12C68 offers hardware protection against inadvertent *STORE* operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$, all externally initiated *STORE* operations will be inhibited.

HSB OPERATION

The Hardware Store Busy pin ($\overline{HSB}$) is an open drain circuit acting as both input and output to perform two different functions. When driven low by the internal chip circuitry it indicates that a *STORE* operation (initiated via any means) is in progress within the chip. When driven low by external circuitry for longer than t_{ASSERT} , the chip will conditionally initiate a *STORE* operation after t_{DELAY} .

READ and *WRITE* operations that are in progress when $\overline{HSB}$ is driven low (either by internal or external circuitry) will be allowed to complete before the *STORE* operation is performed, in the following manner. After $\overline{HSB}$ goes low, the part will continue normal SRAM operations for t_{DELAY} . During t_{DELAY} , a transition on any address or control signal will terminate SRAM operation and cause the *STORE* to commence. Note that if an SRAM write is attempted after $\overline{HSB}$ has been forced low, the write will not occur and the *STORE* operation will begin immediately.

HARDWARE-STORE-BUSY ($\overline{HSB}$) is a high speed, low drive capability bi-directional control line. In order to allow a bank of STK12C68s to perform synchronized *STORE* functions, the $\overline{HSB}$ pin from a number of chips may be connected together. Each chip contains

a small internal current source to pull $\overline{HSB}$ HIGH when it is not being driven low. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to V_{CCX} via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed I_{HSB_OL} at V_{OL} . Do not connect this or any other pull-up to the V_{CAP} node.

If $\overline{HSB}$ is to be connected to external circuits other than other STK12C68s, an external pull-up resistor should be used.

During any *STORE* operation, regardless of how it was initiated, the STK12C68 will continue to drive the HSB pin low, releasing it only when the *STORE* is complete. Upon completion of a *STORE* operation, the part will be disabled until HSB actually goes HIGH.

AUTOMATIC STORE OPERATION

During normal operation, the STK12C68 will draw current from V_{CCX} to charge up a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a *STORE* operation.

Figure 1 shows the proper connection of capacitors for automatic store operation. The charge storage capacitor should have a capacity of at least 100 μ F ($\pm 20\%$) at 6V. Each STK12C68 must have its own 100 μ F capacitor. Each STK12C68 *must* have a high quality, high frequency bypass capacitor of 0.1 μ F connected between V_{CAP} and V_{SS} , using leads and traces that are as short as possible.

If the AutoStore™ function is not required, then V_{CAP} should be tied directly to the power supply and V_{CCX} should be tied to ground. In this mode, *STORE* operations may be triggered through software control or the $\overline{HSB}$ pin. In either event, V_{CAP} (Pin 1) *must* always have a proper bypass capacitor connected to it.

In order to prevent unneeded *STORE* operations, automatic *STOREs* as well as those initiated by externally driving $\overline{HSB}$ LOW will be ignored unless at least one *WRITE* operation has taken place since the most recent *STORE* cycle. Note that if $\overline{HSB}$ is driven low via external circuitry and no *WRITEs* have taken place, the part will

still be disabled until $\overline{\text{HSB}}$ is allowed to return HIGH. Software initiated *STORE* cycles are performed regardless of whether or not a *WRITE* operation has taken place.

PREVENTING AUTOMATIC STORES

The AutoStore™ function can be disabled on the fly by holding $\overline{\text{HSB}}$ HIGH with a driver capable of sourcing 15mA at a VOH of at least 2.2V as it will have to overpower the internal pull-down device that drives $\overline{\text{HSB}}$ low for 50ns at the onset of an AutoStore™. When the STK12C68 is connected for AutoStore™ operation (system V_{CC} connected to V_{CCX} and a 100uF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK12C68 will attempt to pull $\overline{\text{HSB}}$ low; if $\overline{\text{HSB}}$ doesn't actually get below V_{IL} , the part will stop trying to pull $\overline{\text{HSB}}$ LOW and abort the AutoStore™ attempt.

LOW AVERAGE ACTIVE POWER

The STK12C68 has been designed to draw significantly less power when $\overline{\text{E}}$ is LOW (chip enabled) but the access cycle time is longer than 55ns. Figure 2 below

shows the relationship between I_{CC} and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels, over the commercial temperature range. Figure 3 shows the same relationship for WRITE cycles. When $\overline{\text{E}}$ is HIGH, the chip consumes only standby currents, and these plots do not apply.

The cycle time used in Figure 2 corresponds to the length of time from the later of the last address transition or $\overline{\text{E}}$ going LOW to the earlier of $\overline{\text{E}}$ going HIGH or the next address transition. $\overline{\text{W}}$ is assumed to be HIGH, while the state of $\overline{\text{G}}$ does not matter. Additional current is consumed when the address lines change state while $\overline{\text{E}}$ is asserted. The cycle time used in Figure 3 corresponds to the length of time from the later of $\overline{\text{W}}$ or $\overline{\text{E}}$ going LOW to the earlier of $\overline{\text{W}}$ or $\overline{\text{E}}$ going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled ($\overline{\text{E}}$ HIGH); 3) the cycle time for accesses ($\overline{\text{E}}$ LOW); 4) the ratio of reads to writes; 5) the operating temperature and; 6) the V_{CC} level.

4

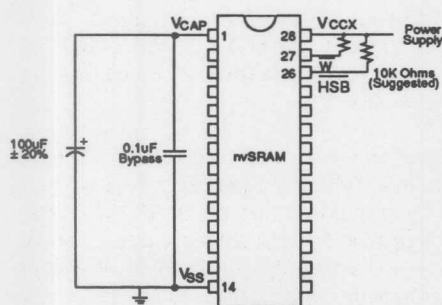


Figure 1. Schematic Diagram

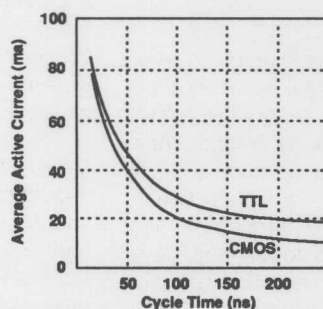


Figure 2. I_{CC} (Max) Reads

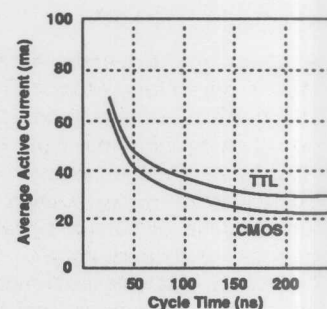


Figure 3. I_{CC} (Max) Writes

Note: Typical at 25° C

ORDERING INFORMATION

STK12C68 - P 35 I

Temperature Range

blank = Commercial (0 - 70 degrees C)

I = Industrial (-40 - 85 degrees C)

Access Time

30 = 30ns

35 = 35ns

45 = 45ns

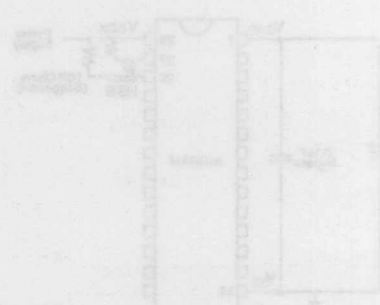
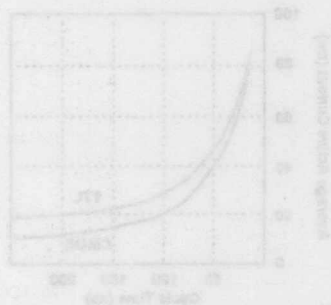
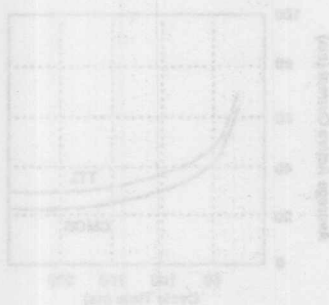
Package

P = Plastic 28 pin 300 mil DIP

W = Plastic 28 pin 600 mil DIP

S = Plastic 28 pin SOIC

C = Ceramic 28 pin 300 mil DIP





STK12C68-M

CMOS nvSRAM

8K x 8 AutoStore™

Nonvolatile Static RAM

MIL-STD-883 / SMD # 5962-94599

FEATURES

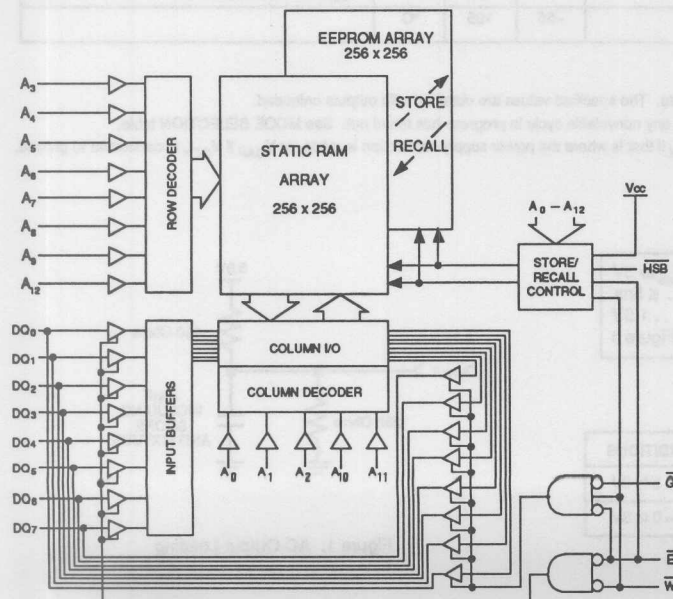
- 35, 45 and 55ns Access Times
- 15 mA I_{CC} at 200ns Access Speed
- Automatic *STORE* to EEPROM on Power Down
- Hardware or Software Initiated *STORE* to EEPROM
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Software Initiated *RECALL* from EEPROM
- Unlimited *RECALL* cycles from EEPROM
- Single $5V \pm 10\%$ Operation
- Available in multiple standard packages

DESCRIPTION

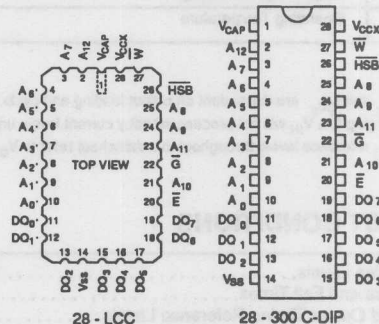
The Simtek STK12C68-M is a fast static RAM (35, 45 and 55ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) take place automatically upon power down using charge stored in an external 100 μF capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on power up. Software sequences may also be used to initiate both *STORE* and *RECALL* operations. A *STORE* can also be initiated via a single pin.

The STK12C68-M is available in the following packages: a 28-pin 300 mil ceramic DIP and 28-pad LCC. Commercial and Industrial temperature devices are also available.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

Pin Name	Description
$A_0 - A_{12}$	Address Inputs
$\bar{W}$	Write Enable
$DQ_0 - DQ_7$	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
V_{CCX}	Power (+5V)
V_{SS}	Ground
V_{CAP}	Capacitor
HSB	Hardware Store/Busy

ABSOLUTE MAXIMUM RATINGS^a

Voltage on typical input relative to V_{SS} -0.6V to 7.0V
 Voltage on DQ_{0-7} and $\bar{Q}$ -0.5V to ($V_{CC}+0.5V$)
 Temperature under bias -55°C to 125°C
 Storage temperature -65°C to 150°C
 Power dissipation 1W
 DC output current 15mA
 (One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

 $(V_{CC} = 5.0V \pm 10\%)^d$

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}^b	Average V_{CC} Current		85 80 75	mA mA mA	$t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ $t_{AVAV} = 55ns$
I_{CC2}	Average V_{CC} Current During STORE		8	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC3}^b	Average V_{CC} Current at $t_{AVAV} = 200ns$		15	mA	$\bar{E} \leq 0.2V$, $W \geq (V_{CC} - 0.2V)$ others $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	Average V_{CC} current during AutoStore™ cycle		4	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}^c	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		35 32 28	mA mA mA	$t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$ $t_{AVAV} = 55ns$ $\bar{E} \geq V_{IH}$; all others cycling
I_{SB2}^c	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		4	mA	$\bar{E} \geq (V_{CC} - 0.2V)$
I_{LK}	Input Leakage Current (Any Input)		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		± 5	μA	$V_{CC} = \max$ $V_{OUT} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC}+5$	V	All Inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS}-5$	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$ except HSB
V_{OL}	Output Logic "0" Voltage		0.4	V	$I_{OUT} = 8mA$ except HSB
T_A	Operating Temperature	-55	125	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d: V_{CC} reference levels throughout this datasheet refer to V_{CCX} if that is where the power supply connection is made, or V_{CAP} if V_{CCX} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels V_{SS} to 3V
 Input Rise and Fall Times $\leq 5ns$
 Input and Output Timing Reference Levels 1.5V
 Output Load See Figure 1

CAPACITANCE^e ($T_A=25^\circ C$, $f=1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

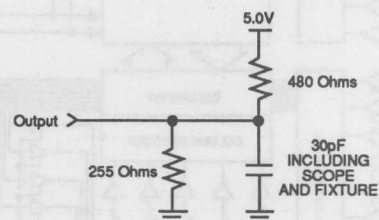


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

READ CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)^d$

NO.	SYMBOLS		PARAMETER	STK12C68-35M		STK12C68-45M		STK12C68-55M		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELOV}	t_{ACS}	Chip Enable Access Time		35		45		55	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	35		45		55		ns
3	t_{AVOV}^g	t_{AA}	Address Access Time		35		45		55	ns
4	t_{GLOV}	t_{OE}	Output Enable to Data Valid		20		25		35	ns
5	t_{AXOX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELOX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHOZ}^h	t_{HZ}	Chip Disable to Output Inactive		17		20		25	ns
8	t_{GLOX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHOZ}^h	t_{OHZ}	Output Disable to Output Inactive		17		20		25	ns
10	t_{ELICCH}^e	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{e,g}$	t_{PS}	Chip Disable to Power Standby		35		45		55	ns

Note c: Bringing $\bar{E} \geq V_{IH}$ will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

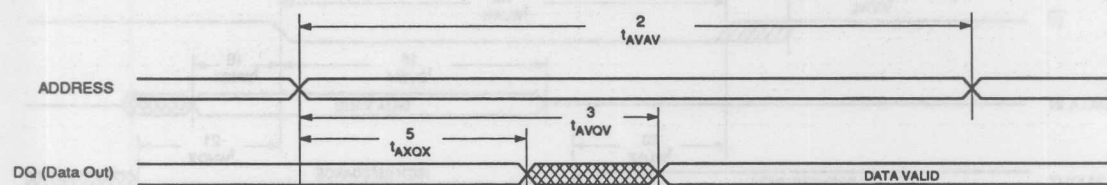
Note e: Parameter guaranteed but not tested.

Note f: For READ CYCLE #1 and #2, $\bar{W}$ is high for entire cycle.

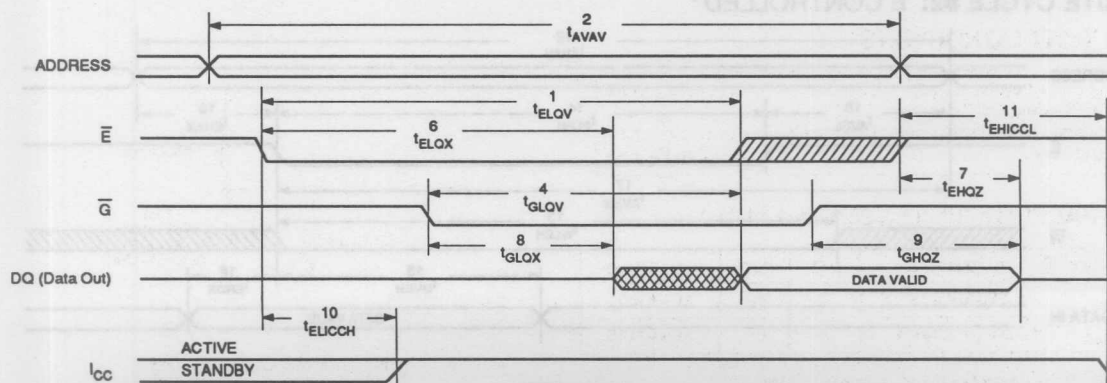
Note g: Device is continuously selected with $\bar{E}$ low and $\bar{G}$ low.

Note h: Measured $\pm 200mV$ from steady state output voltage.

READ CYCLE #1 ^{f,g}



READ CYCLE #2 ^f



WRITE CYCLES #1 & #2

($V_{CC} = 5.0V \pm 10\%$)^d

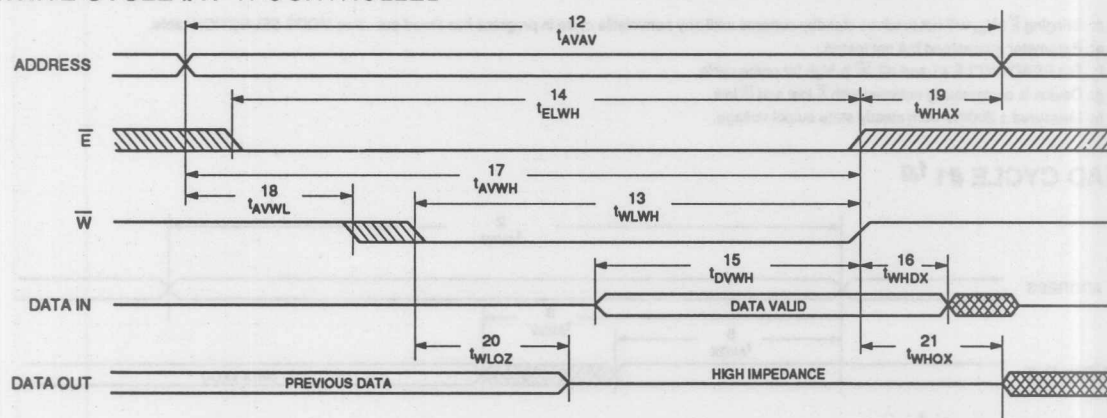
NO.	SYMBOLS			PARAMETE	STK12C68-35M		STK12C68-45M		STK12C68-55M		UNITS
	#1	#2	Alt		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	35		45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	30		35		45		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	30		35		45		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	18		20		25		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	30		35		45		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	$t_{WLOZ}^{h,j}$		t_{WZ}	Write Enable to Output Disable		17		20		25	ns
21	t_{WHOX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note h: Measured $\pm 200mV$ from steady state output voltage.

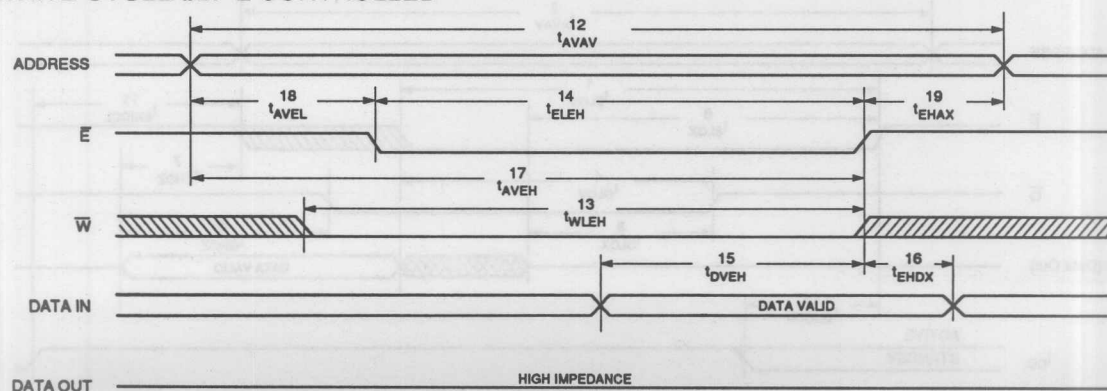
Note i: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ during address transitions.

Note j: If $\bar{W}$ is low when $\bar{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\bar{W}$ CONTROLLEDⁱ



WRITE CYCLE #2: $\bar{E}$ CONTROLLEDⁱ



NONVOLATILE MEMORY OPERATION

MODE SELECTION

E	W	HSB	A ₁₂ - A ₀ (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	I
L	L	H	X	Write SRAM	Input Data	Active	
L	H	H	0000	Read SRAM	Output Data	Active	k,J
			1555	Read SRAM	Output Data		k,J
			0AAA	Read SRAM	Output Data		k,J
			1FFF	Read SRAM	Output Data		k,J
			10F0	Read SRAM	Output Data		k,J
			0F0F	Nonvolatile STORE	Output High Z		k
L	H	H	0000	Read SRAM	Output Data	Active	k,J
			1555	Read SRAM	Output Data		k,J
			0AAA	Read SRAM	Output Data		k,J
			1FFF	Read SRAM	Output Data		k,J
			10F0	Read SRAM	Output Data		k,J
			0F0E	Nonvolatile RECALL	Output High Z		k
X	X	L	X	STORE/Inhibit	Output High Z	I _{CC2} /Standby	m

Note k: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. $\bar{W}$ must be high during all six consecutive cycles. See STORE cycle and RECALL cycle tables and diagrams for further details.

Note l: I/O state assumes that $\bar{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on the state of $\bar{G}$.

Note m: $\bar{HSB}$ Initiated STORE operation actually occurs only if a WRITE has been done since last STORE operation. After the STORE (if any) completes, the part will go into standby mode inhibiting all operation until $\bar{HSB}$ rises.

HARDWARE STORE/RECALL

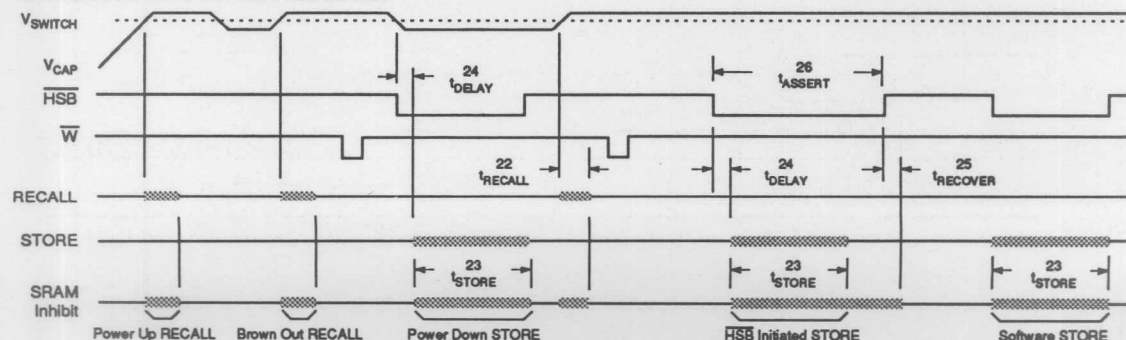
NO.	SYMBOLS	PARAMETER	MIN	MAX	UNITS	NOTES
22	t_{RECALL}	RECALL Cycle Duration		25	μs	Note o
23	t_{STORE}	STORE Cycle Duration		12	ms	$V_{CC} \geq 4.5V$
24	t_{DELAY}	$\bar{HSB}$ Low to Inhibit On	1		μs	
25	$t_{RECOVER}$	$\bar{HSB}$ High to Inhibit Off		300	ns	Note e
26	t_{ASSERT}	External STORE Pulse Width	250		ns	Note e
	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
	I_{HSB_OL}	$\bar{HSB}$ Output Low Current	3		mA	$\bar{HSB} = V_{OL}$, Note e, n
	I_{HSB_OH}	$\bar{HSB}$ Output High Current	5	60	μA	$\bar{HSB} = V_{IL}$, Note e, n

Note e: These parameters guaranteed but not tested.

Note n: $\bar{HSB}$ is an I/O that has a weak internal pullup; it is basically an open drain output. It is meant to allow up to 32 STK12C68-Ms to be ganged together for simultaneous storing. Do not use $\bar{HSB}$ to pullup any external circuitry other than other STK12C68-M $\bar{HSB}$ pins.

Note o: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds V_{SWITCH} . t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

HARDWARE STORE/RECALL



SOFTWARE STORE/RECALL CYCLE

 $(V_{CC} = 5.0V \pm 10\%)^d$

NO.	SYMBOLS		PARAMETER	STK12C68-35M		STK12C68-45M		STK12C68-55M		UNITS
	Std.	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
28	t_{AVAV}	t_{RC}	STORE/RECALL Initiation Cycle Time	35		45		55		ns
29	t_{ELOZ}^p		Chip Enable to Output Inactive		85		85		85	ns
30	t_{AVELN}	t_{AE}	Address Set-up to Chip Enable	0		0		0		ns
31	$t_{ELEHN}^{q,r}$	t_{EP}	Chip Enable Pulse Width	25		35		45		ns
32	t_{EHAXN}	t_{EA}	Chip Disable to Address Change	0		0		0		ns

Note p: Once the software *STORE* or *RECALL* cycle is initiated, it completes automatically, ignoring all inputs.

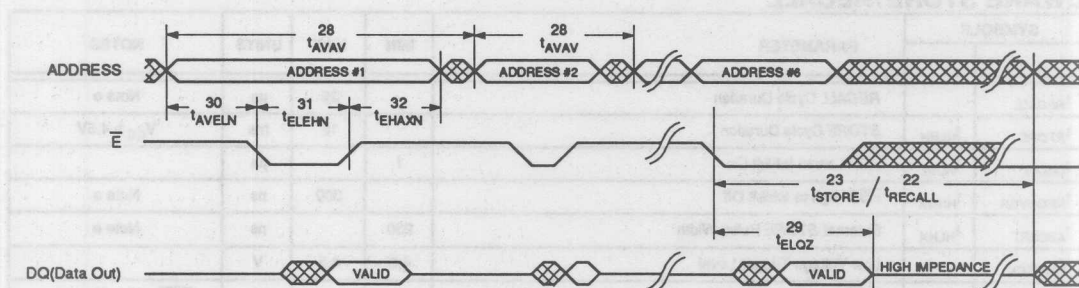
Note q: Noise on the $\bar{E}$ pin may trigger multiple read cycles from the same address and abort the address sequence.

Note r: If the Chip Enable Pulse Width is less than t_{ELOZ} (see READ CYCLE #2) but greater than or equal to t_{ELEHN} , then the data may not be valid at the end of the low pulse, however the *STORE* or *RECALL* will still be initiated.

Note s: $\bar{W}$ must be HIGH when $\bar{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\bar{G}$ may be either HIGH or LOW throughout.

Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK12C68-M performs a *STORE* or *RECALL*.

Note t: $\bar{E}$ must be used to clock in the address sequence for the Software *STORE* and *RECALL* cycles.

SOFTWARE STORE/RECALL CYCLE q,r,t 

DEVICE OPERATION

The STK12C68-M has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via a software sequence or $\overline{\text{HSB}}$ assertion and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH} . *RECALL* operations are automatically initiated upon power-up and whenever the power supply voltage level rises above V_{SWITCH} . *RECALL* cycles may also be initiated by a software sequence.

SRAM READ

The STK12C68-M performs a READ cycle whenever $\overline{\text{E}}$ and $\overline{\text{G}}$ are LOW and $\overline{\text{HSB}}$ and $\overline{\text{W}}$ are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} . If the READ is initiated by $\overline{\text{E}}$ or $\overline{\text{G}}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later. The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{\text{E}}$ or $\overline{\text{G}}$ is brought HIGH or $\overline{\text{W}}$ or $\overline{\text{HSB}}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{\text{E}}$ and $\overline{\text{W}}$ are LOW and $\overline{\text{HSB}}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{\text{E}}$ or $\overline{\text{W}}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{\text{W}}$ controlled WRITE or t_{DVEH} before the end of an $\overline{\text{E}}$ controlled WRITE.

It is recommended that $\overline{\text{G}}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{\text{G}}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{\text{W}}$ goes LOW.

SOFTWARE STORE

The STK12C68-M software *STORE* cycle is initiated by executing sequential READ cycles from six specific

address locations. By relying on READ cycles only, the STK12C68-M implements nonvolatile operation while remaining compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into the nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of addresses is used for *STORE* initiation, it is critical that no other read or write accesses intervene in the sequence or the sequence will be aborted.

To initiate the *STORE* cycle the following READ sequence must be performed:

1. Read address	0000 (hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0F (hex)	Initiate <i>STORE</i> Cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{\text{G}}$ be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

1. Read address	0000(hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0E (hex)	Initiate <i>RECALL</i> Cycle

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the

EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AUTOMATIC RECALL

During power up, or after any low power condition ($V_{CAP} < V_{SWITCH}$), when V_{CAP} exceeds the sense voltage of V_{SWITCH} , a *RECALL* cycle will automatically be initiated. After the initiation of this automatic *RECALL*, if V_{CAP} falls below V_{SWITCH} , then another *RECALL* operation will be performed whenever V_{CAP} again rises above V_{SWITCH} .

If the STK12C68-M is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between W and system V_{CC} .

HARDWARE PROTECT

The STK12C68-M offers hardware protection against inadvertent *STORE* operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$, all externally initiated *STORE* operations will be inhibited.

HSB OPERATION

The Hardware Store Busy pin ($\overline{HSB}$) is an open drain circuit acting as both input and output to perform two different functions. When driven low by the internal chip circuitry it indicates that a *STORE* operation (initiated via any means) is in progress within the chip. When driven low by external circuitry for longer than t_{ASSERT} , the chip will conditionally initiate a *STORE* operation after t_{DELAY} .

READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low (either by internal or external circuitry) will be allowed to complete before the *STORE* operation is performed, in the following manner. After $\overline{HSB}$ goes low, the part will continue normal SRAM operations for t_{DELAY} . During t_{DELAY} , a transition on any address or control signal will terminate SRAM operation and cause the *STORE* to commence. Note that if an SRAM write is attempted after $\overline{HSB}$ has been forced low, the write will not occur and the *STORE* operation will begin immediately.

Hardware-Store-Busy ($\overline{HSB}$) is a high speed, low drive capability bi-directional control line. In order to allow a bank of STK12C68-Ms to perform synchronized *STORE* functions, the $\overline{HSB}$ pin from a number of chips may be

connected together. Each chip contains a small internal current source to pull $\overline{HSB}$ HIGH when it is not being driven low. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to V_{CCX} via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed $I_{\overline{HSB} OL}$ at V_{OL} . Do not connect this or any other pull-up to the V_{CAP} node.

If $\overline{HSB}$ is to be connected to external circuits other than other STK12C68-Ms, an external pull-up resistor should be used.

During any *STORE* operation, regardless of how it was initiated, the STK12C68-M will continue to drive the $\overline{HSB}$ pin low, releasing it only when the *STORE* is complete. Upon completion of a *STORE* operation, the part will be disabled until $\overline{HSB}$ actually goes HIGH.

AUTOMATIC STORE OPERATION

During normal operation, the STK12C68-M will draw current from V_{CCX} to charge up a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a *STORE* operation.

Figure 1 shows the proper connection of capacitors for automatic store operation. The charge storage capacitor should have a capacity of at least 100 μ F ($\pm 20\%$) at 6V. Each STK12C68-M must have its own 100 μ F capacitor. Each STK12C68-M must have a high quality, high frequency bypass capacitor of 0.1 μ F connected between V_{CAP} and V_{SS} , using leads and traces that are as short as possible.

If the *AutoStore*TM function is not required, then V_{CAP} should be tied directly to the power supply and V_{CCX} should be tied to ground. In this mode, *STORE* operations may be triggered through software control or the $\overline{HSB}$ pin. In either event, V_{CAP} (Pin 1) must always have a proper bypass capacitor connected to it.

In order to prevent unneeded *STORE* operations, automatic *STOREs* as well as those initiated by externally driving $\overline{HSB}$ LOW will be ignored unless at least one

WRITE operation has taken place since the most recent *STORE* cycle. Note that if $\overline{\text{HSB}}$ is driven low via external circuitry and no WRITES have taken place, the part will still be disabled until $\overline{\text{HSB}}$ is allowed to return HIGH. Software initiated *STORE* cycles are performed regardless of whether or not a WRITE operation has taken place.

PREVENTING AUTOMATIC STORES

The *AutoStore*TM function can be disabled on the fly by holding $\overline{\text{HSB}}$ HIGH with a driver capable of sourcing 15mA at a VOH of at least 2.2V as it will have to overpower the internal pull-down device that drives $\overline{\text{HSB}}$ low for 50ns at the onset of an *AutoStore*TM. When the STK12C68-M is connected for *AutoStore*TM operation (system V_{CC} connected to V_{CCX} and a 100uF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK12C68 will attempt to pull $\overline{\text{HSB}}$ LOW; if $\overline{\text{HSB}}$ doesn't actually get below V_{IL} , the part will stop trying to pull $\overline{\text{HSB}}$ LOW and abort the *AutoStore*TM attempt.

LOW AVERAGE ACTIVE POWER

The STK12C68-M has been designed to draw significantly less power when $\overline{\text{E}}$ is LOW (chip enabled) but the

access cycle time is longer than 55ns. *Figure 2* below shows the relationship between I_{CC} and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels, over the commercial temperature range. *Figure 3* shows the same relationship for WRITE cycles. When $\overline{\text{E}}$ is HIGH, the chip consumes only standby currents, and these plots do not apply.

The cycle time used in *Figure 2* corresponds to the length of time from the later of the last address transition or $\overline{\text{E}}$ going LOW to the earlier of $\overline{\text{E}}$ going HIGH or the next address transition. $\overline{\text{W}}$ is assumed to be HIGH, while the state of $\overline{\text{G}}$ does not matter. Additional current is consumed when the address lines change state while $\overline{\text{E}}$ is asserted. The cycle time used in *Figure 3* corresponds to the length of time from the later of $\overline{\text{W}}$ or $\overline{\text{E}}$ going LOW to the earlier of $\overline{\text{W}}$ or $\overline{\text{E}}$ going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled ($\overline{\text{E}}$ HIGH); 3) the cycle time for accesses ($\overline{\text{E}}$ LOW); 4) the ratio of reads to writes; 5) the operating temperature and; 6) the V_{CC} level.

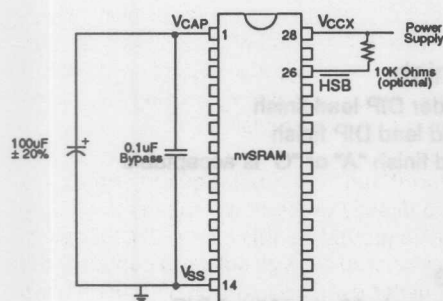


Figure 1
Schematic Diagram

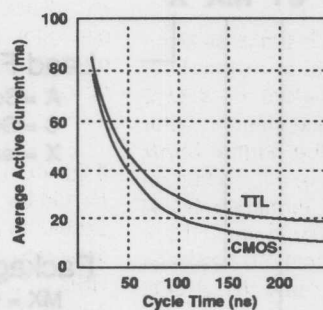


Figure 2
 I_{CC} (Max) Reads

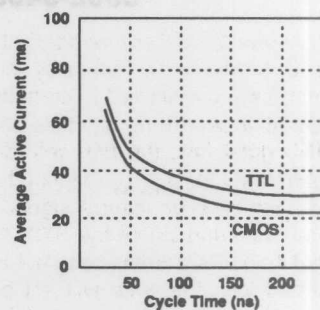


Figure 3
 I_{CC} (Max) Writes

Note: Typical at 25° C

ORDERING INFORMATION

STK12C68 - 5 C 35 M

Temperature Range

M = Military (-55 to 125 degrees C)

Access Time

35 = 35ns

45 = 45ns

55 = 55ns

Package

C = Ceramic 28 pin 300-mil DIP with gold lead finish

K = Ceramic 28 pin 300-mil DIP with solder DIP finish

L = Ceramic 28 pin LCC

Retention / Endurance

10 years / 100,000 cycles

5962-94599 01 MX X

Lead Finish

A = Solder DIP lead finish

C = Gold lead DIP finish

X = lead finish "A" or "C" is acceptable

Package

MX = Ceramic 28 pin 300-mil DIP

MY = Ceramic 28 pin LCC

Access Time

01 = 55ns

02 = 45ns

03 = 35ns

256 kilobit nvSRAM Products 5



SIMTEK

STK11C88

32K x 8 nvSRAM

High Performance CMOS

Nonvolatile Static RAM

PRELIMINARY

FEATURES

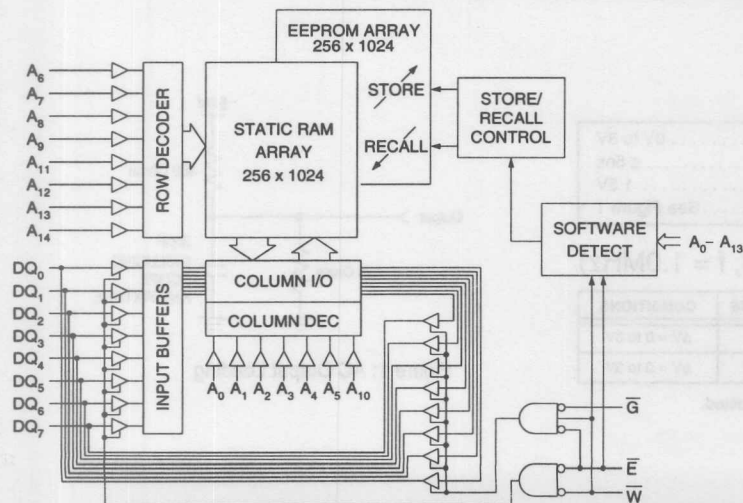
- 25ns, 35ns and 45ns Access Times
- Store to EEPROM Initiated by Software
- Recall to SRAM Initiated by Software or Power Restore
- 25mA I_{CC} at 200ns Cycle Time
- Unlimited Recalls from EEPROM to SRAM
- 100,000 Store Cycles to EEPROM
- 10 Year Data Retention in EEPROM
- Commercial and Industrial Temp. Ranges
- 28 Pin 600 mil PDIP package

DESCRIPTION

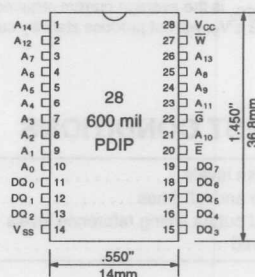
The Simtek STK11C88 is a fast static RAM with a nonvolatile, electrically-erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation), or from EEPROM to SRAM (the *RECALL* operation) also take place using a software sequence. Transfers from the EEPROM to the SRAM (the *RECALL* operation) also take place automatically on restoration of power.

5

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A ₀ - A ₁₄	Address Inputs
$\bar{W}$	Write Enable
DQ ₀ - DQ ₇	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

STK11C88

ABSOLUTE MAXIMUM RATINGS^a

Voltage on input relative to V_{SS}	-0.6V to ($V_{CC} + 0.5V$)
Voltage on DQ_0	-0.5V to ($V_{CC} + 0.5V$)
Temperature under bias	-55°C to 125°C
Storage temperature	-65°C to 150°C
Power dissipation	1W
DC output current	15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average Current		150 130 110		165 145 125	mA	$t_{AVAV} = 25ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$
I_{CC2}^c	Average Current During STORE		6		7	mA	All inputs Don't Care, $V_{CC} = \max$
I_{CC3}^b	Average V_{CC} Current at $t_{AVAV} = 200ns$		25		25	mA	$\bar{W} \geq (V_{CC} - 0.2V)$ All others cycling, CMOS levels
I_{SB1}^d	Average Current (Standby, Cycling TTL Input Levels)		37 33 30		39 35 32	mA	$t_{AVAV} = 25ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 35ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 45ns, \bar{E} \geq V_{IH}$
I_{SB2}^d	Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		± 1		± 1	μA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC} , $\bar{E}$ or $\bar{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC} + .5$	2.2	$V_{CC} + .5$	V	All inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS} - .5$	0.8	$V_{SS} - .5$	0.8	V	All inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: I_{CC2} is the average current required for the duration of the STORE cycle (t_{STORE}).

Note d: $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input pulse levels	0V to 3V
Input rise and fall times	$\leq 5ns$
Input and output timing reference levels	1.5V
Output load	See Figure 1

CAPACITANCE^e ($T_A = 25^\circ C$, $f = 1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

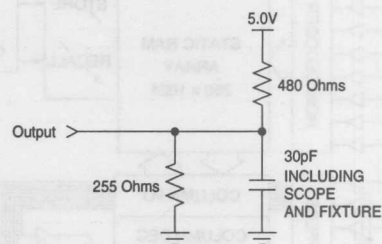
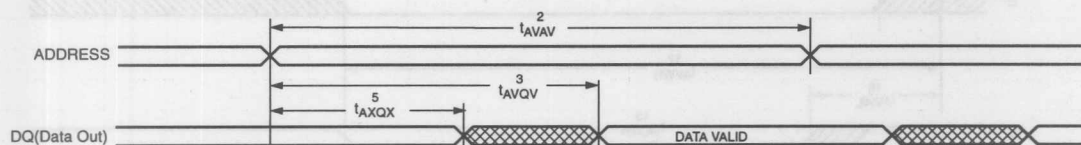
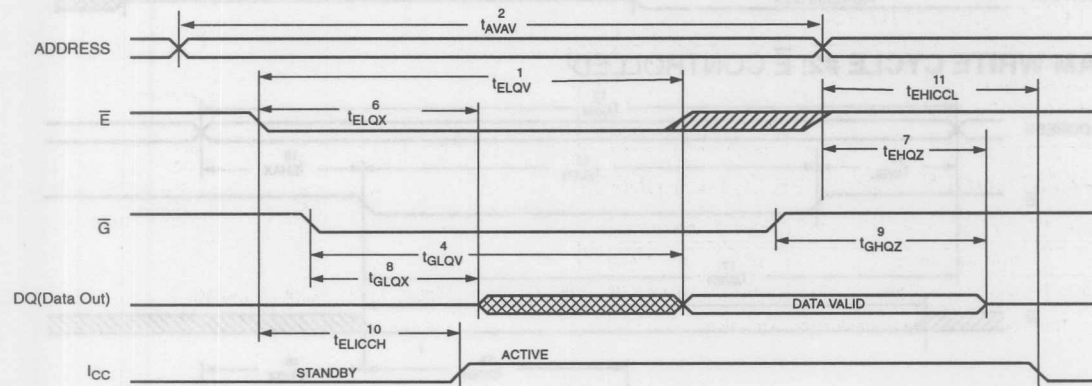


Figure 1: AC Output Loading

SRAM READ CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK11C88-25		STK11C88-35		STK11C88-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}^1	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}^2	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}^3	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}^5	t_{OH}	Output Hold After Address Change	3		3		3		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHOZ}^h	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHOZ}^h	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}^e	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{d,e}$	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note f: $\overline{W}$ must be high during SRAM read cycles and low during SRAM write cycles.Note g: I/O state assumes $\overline{E}$ and $\overline{G} < V_{IL}$ and $W > V_{IH}$; device is continuously selected.Note h: Measured $\pm 200mV$ from steady state output voltageSRAM READ CYCLE #1 (Address Controlled)^{f, g}SRAM READ CYCLE #2 ($\overline{E}$ Controlled)^f

STK11C88

SRAM WRITE CYCLES #1 & #2

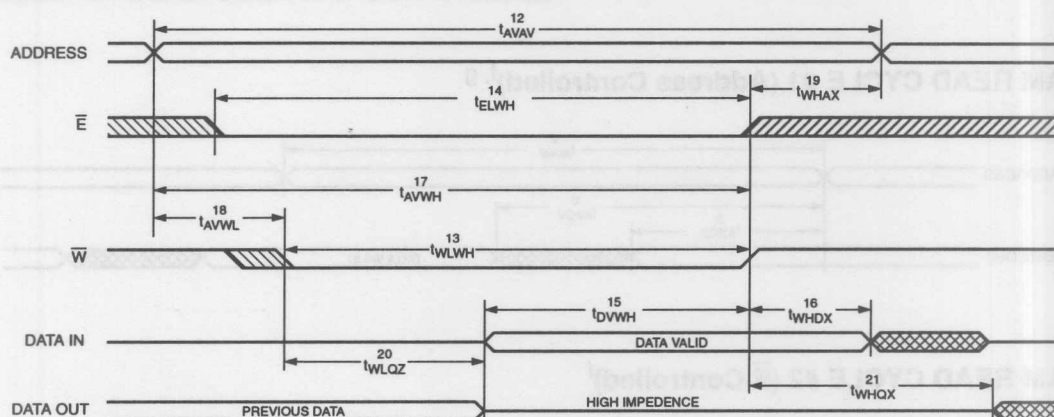
($V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOLS			PARAMETER	STK11C88-25		STK11C88-35		STK11C88-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	$t_{WLOZ}^{h,i}$		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

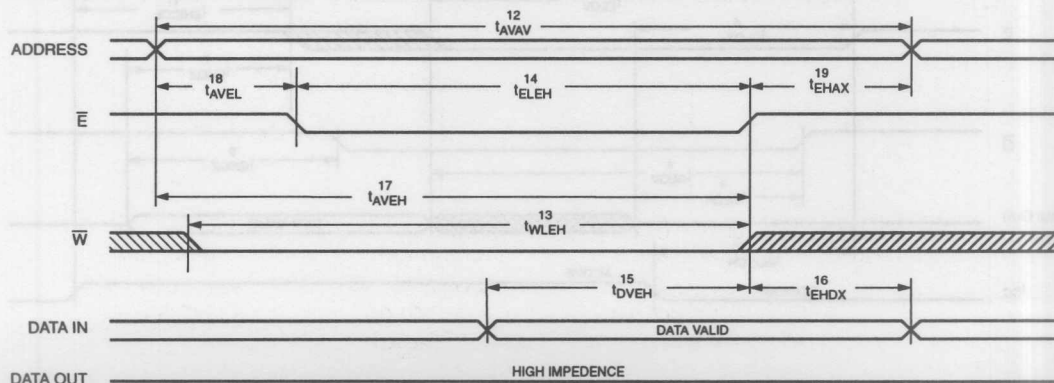
Note i: If $\bar{W}$ is low when $\bar{E}$ goes low the outputs remain in the high impedance state.

Note j: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ during address transitions.

SRAM WRITE CYCLE #1: $\bar{W}$ CONTROLLED^j



SRAM WRITE CYCLE #2: $\bar{E}$ CONTROLLED^j



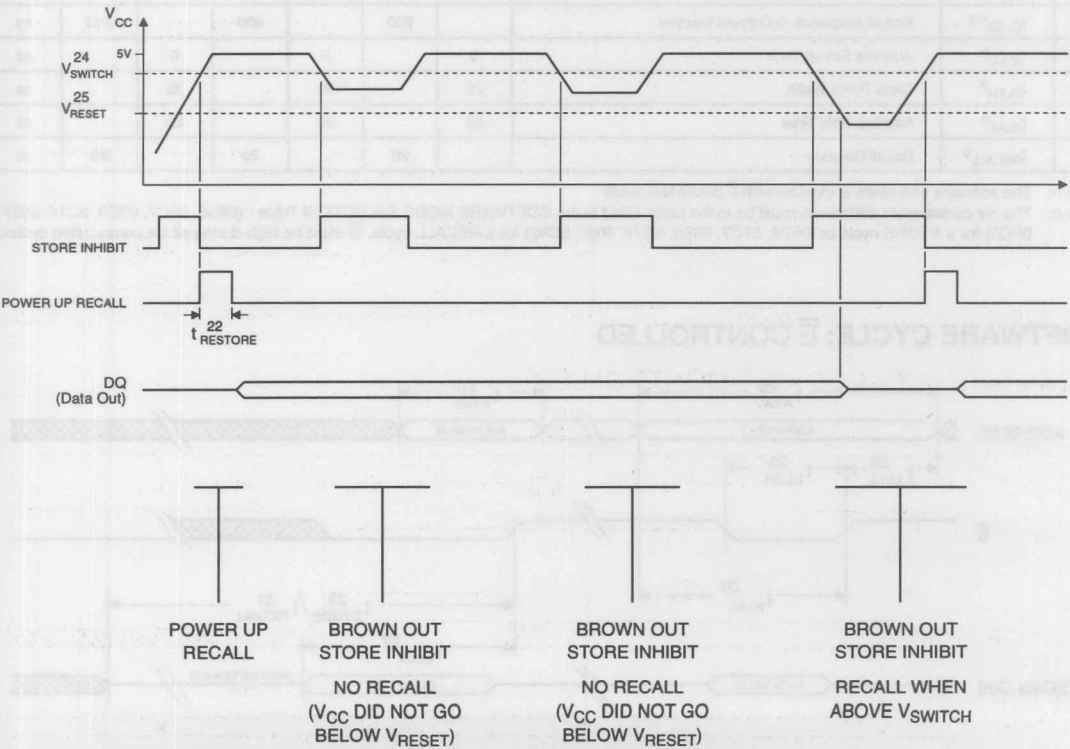
STORE INHIBIT / POWER-UP RECALL

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK11C88		UNITS	NOTES
	Standard		MIN	MAX		
22	t _{RESTORE}	Power-Up RECALL Duration		550	μs	k
23	t _{STORE}	STORE Cycle Duration		10	ms	
24	V _{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
25	V _{RESET}	Low Voltage Reset Level		3.6	V	

Note k: t_{RESTORE} starts from the time V_{CC} rises above V_{SWITCH}.

STORE INHIBIT / POWER-UP RECALL



SOFTWARE MODE SELECTION

$\bar{E}$	$\bar{W}$	A ₁₃ - A ₀ (hex)	MODE	IO	NOTES
L	H	0E38	Read SRAM	Output data	l,m
		31C7	Read SRAM	Output data	
		03E0	Read SRAM	Output data	
		3C1F	Read SRAM	Output data	
		303F	Read SRAM	Output data	
		0FC0	Nonvolatile <i>STORE</i>	Output high Z	
L	H	0E38	Read SRAM	Output data	l,m
		31C7	Read SRAM	Output data	
		03E0	Read SRAM	Output data	
		3C1F	Read SRAM	Output data	
		303F	Read SRAM	Output data	
		0C63	Nonvolatile <i>RECALL</i>	Output high Z	

Note l: The six consecutive addresses must be in order listed. $\bar{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

Note m: While there are 15 addresses on the STK11C88, only the lower 14 are used to control software modes.

SOFTWARE CYCLES #1 & #2^{n,o}

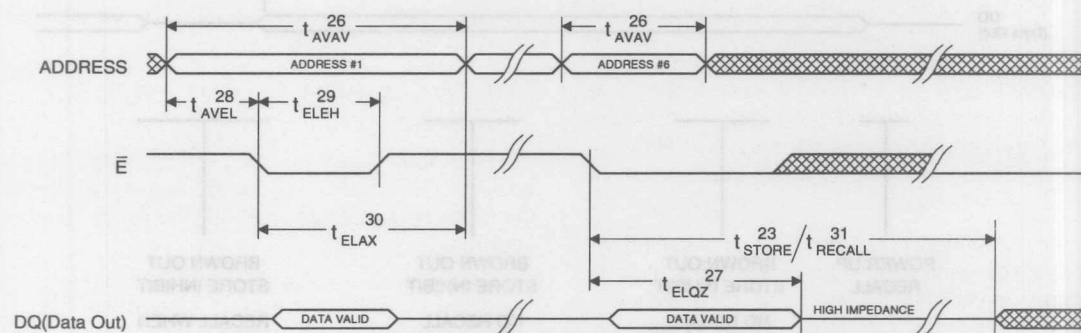
(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK11C88-25		STK11C88-35		STK11C88-45		UNITS
	#1		MIN	MAX	MIN	MAX	MIN	MAX	
26	t _{AVAV}	STORE/RECALL initiation cycle time	25		35		45		ns
27	t _{ELQZ} ^{n,g}	End of Sequence to Outputs Inactive		600		600		600	ns
28	t _{AVEL} ⁿ	Address Set-up Time	0		0		0		ns
29	t _{ELEH} ⁿ	Clock Pulse Width	20		25		30		ns
30	t _{ELAX} ⁿ	Address Hold Time	20		20		20		ns
31	t _{RECALL} ^g	Recall Duration		20		20		20	μs

Note n: The software sequence is clocked with $\bar{E}$ controlled reads

Note o: The six consecutive addresses must be in the order listed in the SOFTWARE MODE SELECTION Table - (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a STORE cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a RECALL cycle. $\bar{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE: $\bar{E}$ CONTROLLED



DEVICE OPERATION

The STK11C88 is a versatile memory chip that provides several modes of operation. The STK11C88 can operate as a standard 32K x 8 SRAM. It has a 32K x 8 EEPROM shadow to which the SRAM information can be copied or from which the SRAM can be updated in nonvolatile mode.

NOISE CONSIDERATIONS

Note that the STK11C88 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 μ F connected between DUT V_{CC} and V_{SS} , using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK11C88 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

SOFTWARE NONVOLATILE STORE

The STK11C88 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

- | | | |
|-----------------|------------|----------------------|
| 1. Read address | 0E38 (hex) | Valid READ |
| 2. Read address | 31C7 (hex) | Valid READ |
| 3. Read address | 03E0 (hex) | Valid READ |
| 4. Read address | 3C1F (hex) | Valid READ |
| 5. Read address | 303F (hex) | Valid READ |
| 6. Read address | 0FC0 (hex) | Initiate STORE cycle |

The software sequence is clocked with $\overline{E}$ controlled reads.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed:

- | | | |
|-----------------|------------|-----------------------|
| 1. Read address | 0E38 (hex) | Valid READ |
| 2. Read address | 31C7 (hex) | Valid READ |
| 3. Read address | 03E0 (hex) | Valid READ |
| 4. Read address | 3C1F (hex) | Valid READ |
| 5. Read address | 303F (hex) | Valid READ |
| 6. Read address | 0C63 (hex) | Initiate RECALL cycle |

STK11C88

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

POWER UP RECALL

During power up, or after any low power condition ($V_{\text{CC}} < V_{\text{RESET}}$) an internal recall request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH} , a RECALL cycle will automatically be initiated and will take t_{RESTORE} to complete.

HARDWARE PROTECT

The STK11C88 offers hardware protection against inadvertent STORE operation during low voltage

conditions. When $V_{\text{CC}} < V_{\text{SWITCH}}$ all Software STORE operations will be inhibited.

LOW AVERAGE ACTIVE POWER

The STK11C88 draws significantly less current when it is cycled at times longer than 30ns. Figure 2, below, shows the relationship between I_{CC} and READ cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, $V_{\text{CC}} = 5.5\text{V}$, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK11C88 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READ's to WRITE's; 5) the operating temperature; 6) the V_{CC} level and; 7) I/O loading.

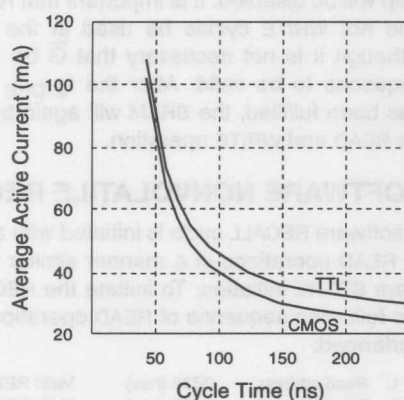


Fig 2: I_{CC} (max) Reads

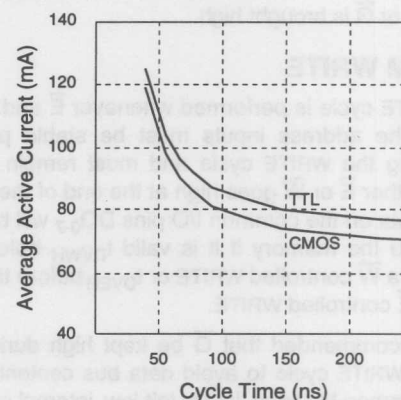


Fig 3: I_{CC} (Max) Writes

ORDERING INFORMATION

STK11C88 - W 25 I



Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

W = Plastic 28 pin 600 mil PDIP

ORDERING INFORMATION

Temperature Range
 Blank = Commercial (0 to 70 degrees C)
 I = Industrial (-45 to 85 degrees C)

Access Time

25 = 25ms
 35 = 35ms
 45 = 45ms

Package

W = Plastic 28 pin 500 mil PDIP

STK1088 - W 25 I





STK12C88

32K x 8 *AutoStore*™ nvSRAM

High Performance CMOS

Nonvolatile Static RAM

PRELIMINARY

FEATURES

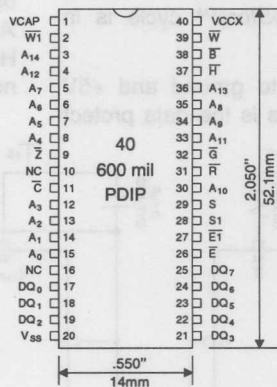
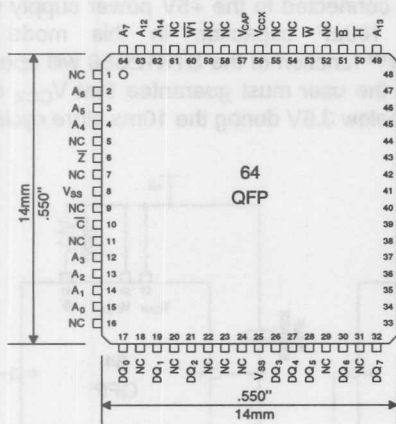
- 25ns, 35ns and 45ns Access Times
- Store to EEPROM Initiated by Hardware, Software or *AutoStore*™ on Power Down
- Recall to SRAM Initiated by Hardware Reset, Software or Power Restore
- "Hands-off" Store with 100μF Capacitor
- Low Power Sleep Mode: $I_{CC} < 10\mu A$
- 25mA I_{CC} at 200ns Cycle Time
- Multiple Select and Enable Pins for Flexible Interface to Processors
- Separate Strobe Input for Software Control
- Unlimited Recalls from EEPROM to SRAM
- 100,000 Store Cycles to EEPROM
- 10 Year Data Retention in EEPROM
- Commercial and Industrial Temp. Ranges
- 64 Pin PQFP and 40 Pin 600 mil PDIP Packages

DESCRIPTION

The Simtek STK12C88 is a fast static RAM with a nonvolatile, electrically-erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down using charge stored in an external capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of STORE and RECALL cycles can also be controlled by separate input pins or by entering control sequences on the SRAM inputs. Hardware reset and low power SLEEP mode functions are included.

5

PACKAGE DIAGRAMS

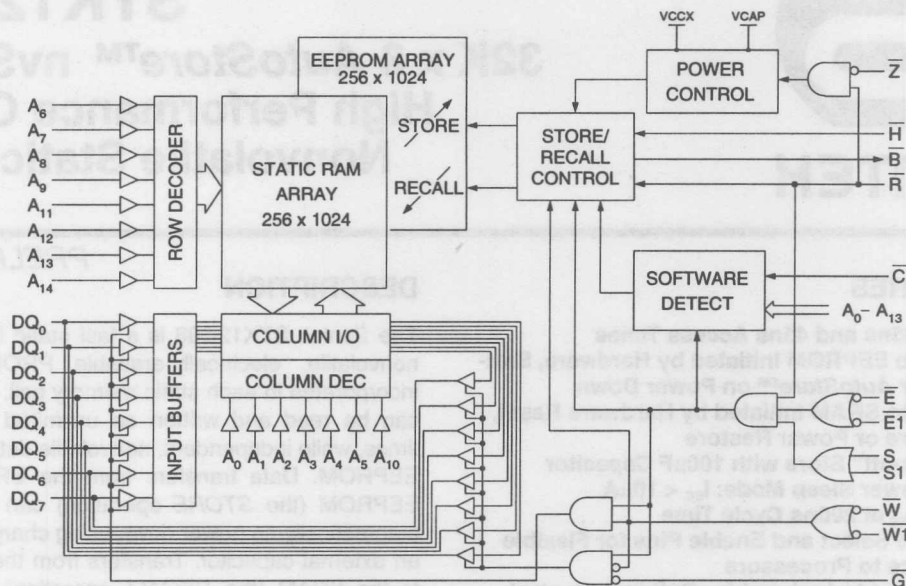


PIN NAMES

$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data In/Out
$\bar{E}, \bar{E}_1$	Chip Enables (Low)
S, S1	Chip Selects (High)
$\bar{W}, \bar{W}_1$	Write Enables
$\bar{G}$	Output Enable
$\bar{H}$	Hardware Store
$\bar{R}$	Hardware Reset
$\bar{B}$	Store Busy
$\bar{C}$	Software Clock
$\bar{Z}$	Sleep Mode Enable
VCCX	Power (+5V)
V _{CAP}	Capacitor
V _{SS}	Ground

STK12C88

BLOCK DIAGRAM



POWER SUPPLY CONNECTION OPTIONS

The STK12C88 can be powered in three modes. In the normal mode, 5V is supplied to V_{CCX} and a 100μF capacitor is connected to the V_{CAP} terminal, as shown in Figure 1. This datasheet is written assuming that this configuration is used so power supply specifications will refer to V_{CCX}. An optional pull up resistor is shown connected to $\bar{B}$. This is used to signal that the *AutoStore*[™] cycle is in progress.

Optionally, V_{CCX} can be tied to ground and +5V applied to V_{CAP} (Figure 2). This is the data protect

mode in which the *AutoStore*[™] function is disabled. If the STK12C88 is operated in this configuration, references to V_{CCX} should be changed to V_{CAP} throughout this data sheet.

In system power mode (Figure 3) both V_{CCX} and V_{CAP} are connected to the +5V power supply without the 100μF capacitor. In this mode the *AutoStore*[™] function of the STK12C88 will operate. However, the user must guarantee that V_{CCX} does not drop below 3.6V during the 10ms store cycle.

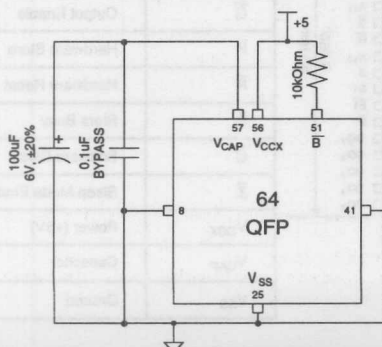


Figure 1: *AutoStore*[™] Mode

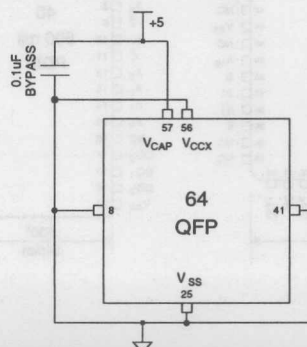


Figure 2: Data Protect Mode

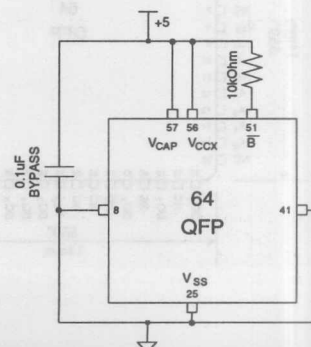


Figure 3: System Power Mode

MULTIPLE CONTROL INPUTS

The STK12C88 provides dual control pins for each of the primary SRAM control functions, chip enable ($\bar{E}$), chip select (S) and write enable ($\bar{W}$). The secondary input carries the suffix "1", e.g. $\bar{E}1$. These multiple inputs are provided for ease of interface to various processors and control chips. They allow such functions as data and program access to the same STK12C88 chip and independent control of the nonvolatile software sequences.

Either control pin from each pair may be used interchangeably. For the sake of brevity, this datasheet references only the non-suffix input per pair but all AC and DC specifications apply to both.

Logical AND and OR chip selection is possible using

the chip select and chip enable input pairs. To select the chip, S or S1 must be active HIGH and $\bar{E}$ or $\bar{E}1$ must be active LOW. The Boolean definition is $(\bar{E} \cdot \bar{E}1) \cdot (S + S1)$. The SRAM write function is enabled when $\bar{W}$ or $\bar{W}1$ is active low.

An additional input, $\bar{C}$, is provided for more flexible control of the software modes (see software mode selection table). The software sequence can be clocked with $\bar{E}$ or S controlled reads assuming $\bar{C}$ is low, or clocked by $\bar{C}$ if the STK12C88 is already enabled. The Boolean definition of the software clock function is $\bar{C} \cdot (\bar{E} \cdot \bar{E}1) \cdot (S + S1)$. If the additional control is not needed the $\bar{C}$ pin can be tied to 0V. The software clock, $\bar{C}$, has no effect on SRAM cycles.

HARDWARE MODE SELECTION

$\bar{E}$	S	$\bar{W}$	$\bar{G}$	$\bar{H}$	$\bar{Z}$	$\bar{R}$	MODE	POWER	NOTES
H	X	X	X	H	H	H	Not selected	Standby	a
X	L	X	X	H	H	H	Not selected	Standby	a
L	H	H	L	H	H	H	Read RAM	Active	
L	H	L	X	H	H	H	Write RAM	Active	b
X	X	X	X	L	X	X	Nonvolatile STORE	I_{CC2}	c, d
X	X	X	X	X	L	H	SLEEP mode	I_{ZZ}	
X	X	X	X	X	X	L	Hardware RESET / RECALL	Standby	

SOFTWARE MODE SELECTION

$\bar{E}$	S	$\bar{C}$	$\bar{W}$	$\bar{R}$	$\bar{H}$	$\bar{Z}$	A ₁₃ - A ₀ (hex)	MODE	I/O	NOTES
L	H	H	H	H	H	H	X	Read SRAM Software Disabled	Output data	
L	H	L	H	H	H	H	0E38 31C7 03E0 3C1F 303F 0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output data Output data Output data Output data Output data Output high Z	e, f
L	H	L	H	H	H	H	0E38 31C7 03E0 3C1F 303F 0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output data Output data Output data Output data Output data Output high Z	e, f

Note a: The Boolean expression of chip selection is $(\bar{E} \cdot \bar{E}1) \cdot (S + S1)$.

Note b: Assuming the chip is selected, the Boolean expression for write selection is $(\bar{W} \cdot \bar{W}1)$.

Note c: $\bar{H}$ store operation occurs only if an SRAM write has been done since the last nonvolatile cycle. After the store (if any) completes the part will go into standby mode inhibiting all operations until $\bar{H}$ rises.

Note d: $\bar{R}$ must be held high for t_{HLRL} after $\bar{H}$ otherwise the store cycle may be aborted by the reset request.

Note e: The six consecutive addresses must be in order listed. $\bar{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

Note f: While there are 15 addresses on the STK12C88, only the lower 14 are used to control software modes.

STK12C88

ABSOLUTE MAXIMUM RATINGS⁹

Voltage on input relative to V_{SS} -0.5V to ($V_{CCX} + 0.5V$)
 Voltage on DQ_0 or $\bar{B}$ -0.5V to ($V_{CCX} + 0.5V$)
 Temperature under bias -55°C to 125°C
 Storage temperature -65°C to 150°C
 Power dissipation 1W
 DC output current (1 output at a time, 1s duration) 15mA

Note g: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CCX} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^h	Average V_{CCX} Current		155 135 115		170 150 130	mA	$t_{AVAV} = 25ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$
I_{CC2}^i	Average V_{CCX} Current During STORE		6		7	mA	All inputs Don't Care
I_{CC3}^h	Average V_{CCX} Current at $t_{AVAV} = 200ns$		25		25	mA	$\bar{W} \geq (V_{CCX} - 0.2V)$ All others cycling, CMOS levels
I_{CC4}^i	Average V_{CAP} Current During AutoStore™ Cycle		4		4	mA	All inputs Don't Care
I_{SB1}^i	Average V_{CCX} Current (Standby, Cycling TTL Input Levels)		40 36 33		42 38 35	mA	$t_{AVAV} = 25ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 35ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 45ns, \bar{E} \geq V_{IH}$
I_{SB2}^j	V_{CCX} Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\bar{E} \geq (V_{CCX} - 0.2V)$ or $S \leq 0.2V$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CCX} - 0.2V)$
I_{ZZ}	V_{CCX} Current During Sleep Mode		10		10	μA	$\bar{Z} \leq 0.2V; \bar{R} \geq (V_{CCX} - 0.2V)$; all others Don't Care. Typical current = $2\mu A$
I_{ILK}	Input Leakage Current		± 1		± 1	μA	$V_{CCX} = \max$ $V_{IN} = V_{SS}$ to V_{CCX}
I_{OLK}	Off-State Output Leakage Current		± 1		± 1	μA	$V_{CCX} = \max$ $V_{IN} = V_{SS}$ to V_{CCX} , $\bar{E}$ or $\bar{G} \geq V_{IH}$ or $S \leq V_{IL}$
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CCX} + .5$	2.2	$V_{CCX} + .5$	V	All inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS} - .5$	0.8	$V_{SS} - .5$	0.8	V	All inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
V_{BL}	Logic "0" Voltage on $\bar{B}$ Output		0.4		0.4	V	$I_{OUT} = 3mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note h: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note i: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective STORE cycles (t_{STORE}).

Note j: $\bar{E} \geq V_{IH}$ or $S \leq V_{IL}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input pulse levels 0V to 3V
 Input rise and fall times $\leq 5ns$
 Input and output timing reference levels 1.5V
 Output load See Figure 4

CAPACITANCE^k ($T_A = 25^\circ C, f = 1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output capacitance	7	pF	$\Delta V = 0$ to 3V

Note k: These parameters are guaranteed but not tested.

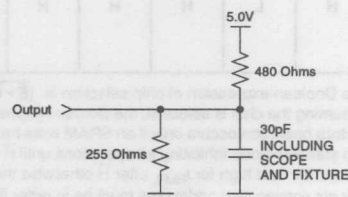
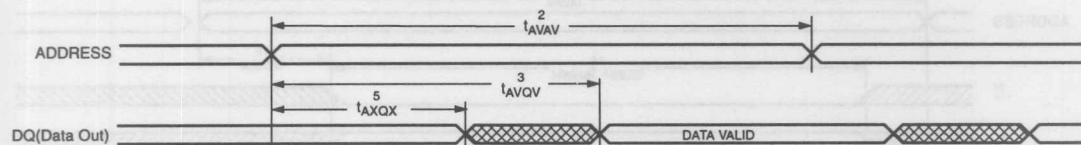
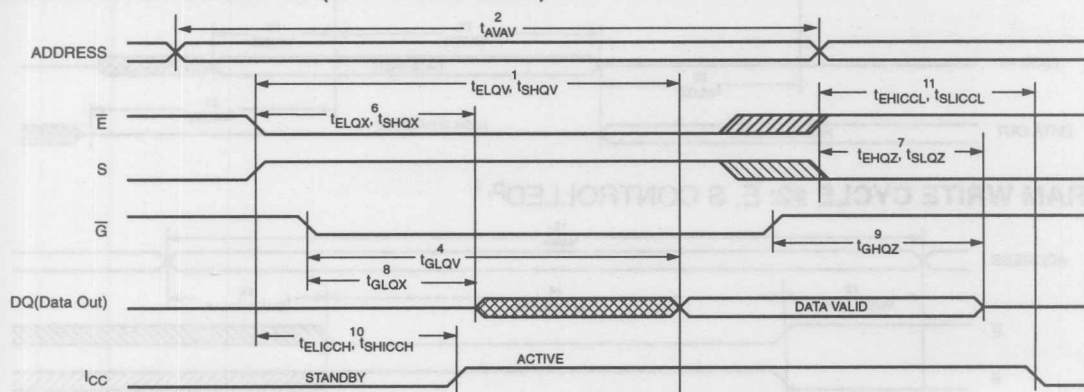


Figure 4: AC Output Loading

SRAM READ CYCLES #1 & #2

 $(V_{CCX} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK12C88-25		STK12C88-35		STK12C88-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}^1, t_{SHQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}^1	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}^m	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}^m	t_{OH}	Output Hold After Address Change	3		3		3		ns
6	t_{ELQX}, t_{SHQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}, t_{SLOZ}^n	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}^n	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}, t_{SHICCH}^k	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}, t_{SLICCL}^k	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

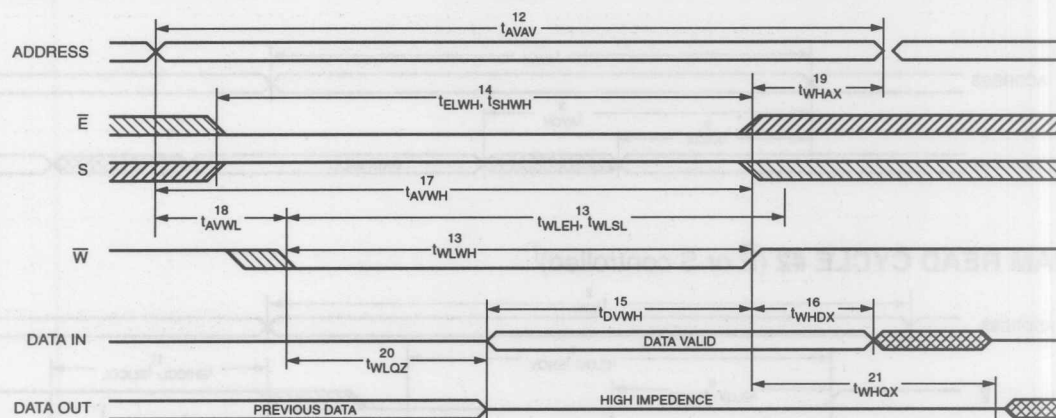
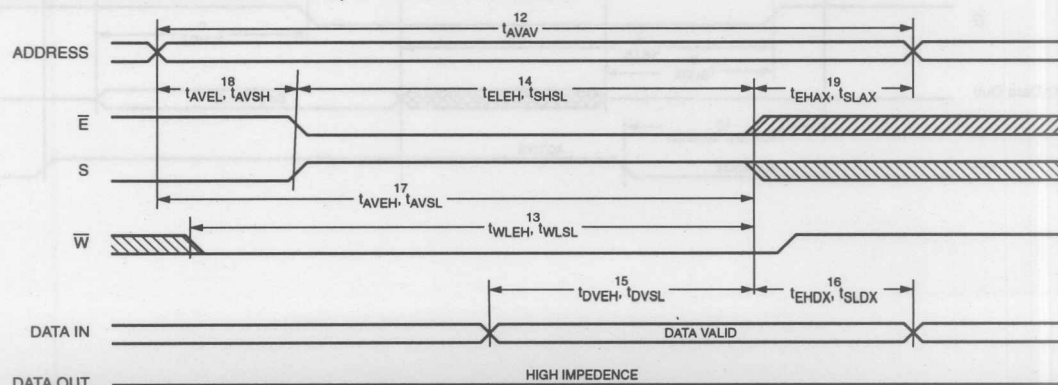
Note l: $\bar{W}$, $\bar{H}$, $\bar{R}$ and $\bar{Z}$ must be high during SRAM read and write cycles.Note m: Device is continuously selected with $\bar{E}$ and $\bar{G}$ both low and S high.Note n: Measured $\pm 200mV$ from steady state output voltageSRAM READ CYCLE #1 (Address Controlled)^{l, m}SRAM READ CYCLE #2 ($\bar{E}$ or S controlled)^l

SRAM WRITE CYCLES #1 & #2
 $(V_{CCX} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	STK12C88-25		STK12C88-35		STK12C88-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}, t_{WLSL}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}, t_{SHEH}	t_{ELEH}, t_{SHSL}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}, t_{DVSL}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}, t_{SLDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}, t_{AVSL}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}, t_{AVSH}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}, t_{SLAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	$t_{WLOZ}^{n,o}$		t_{WZ}	Write Dnable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note o: If $\bar{W}$ is low when either $\bar{E}$ goes low or S goes high, the outputs remain in the high impedance state.

Note p: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ or S must be $\leq V_{IL}$ during address transitions.

SRAM WRITE CYCLE #1: $\bar{W}$ CONTROLLED^{p, l}

SRAM WRITE CYCLE #2: $\bar{E}$, S CONTROLLED^{p, l}


HARDWARE STORE CYCLE

($V_{CCX} = 5.0V \pm 10\%$)

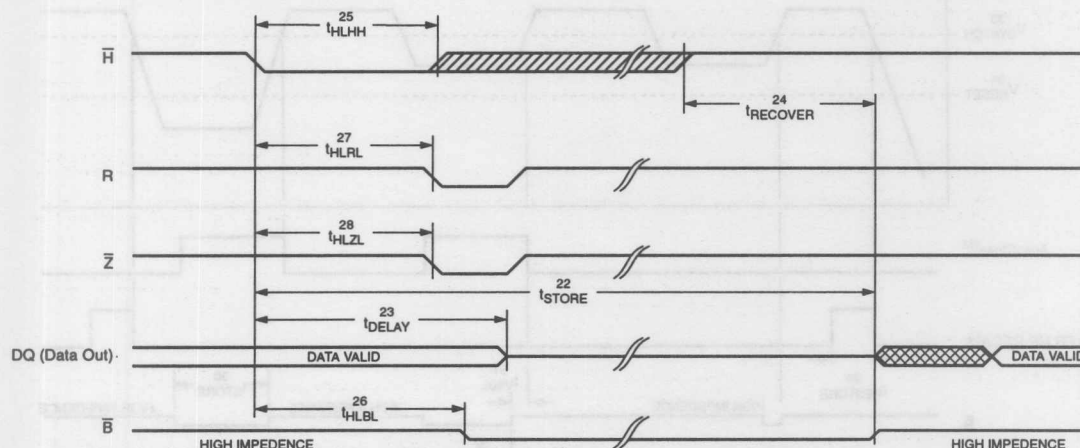
NO.	SYMBOLS		PARAMETER	STK12C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t_{STORE}	t_{HLBZ}	STORE Cycle Duration		10	ms	n, q
23	t_{DELAY}	t_{HLOZ}	Time allowed to Complete SRAM Cycle	1		μs	n, r
24	$t_{RECOVER}$	t_{HHQX}	Hardware Store High to Inhibit Off		200	ns	q, s
25	t_{HLHH}		Hardware Store Pulse Width	20		ns	
26	t_{HLBL}		Hardware Store Low to Store Busy		300	ns	
27	t_{HLRL}		Hardware Store Set-up to Reset	300		ns	
28	t_{HLZL}		Hardware Store Set-up to Sleep	10		ns	

Note q: $\bar{E}$ and $\bar{G}$ low and S, R, $\bar{Z}$ and $\bar{H}$ high for output behavior.

Note r: $\bar{E}$ and $\bar{G}$ low and S, R, and $\bar{Z}$ high for output behavior.

Note s: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE STORE CYCLE

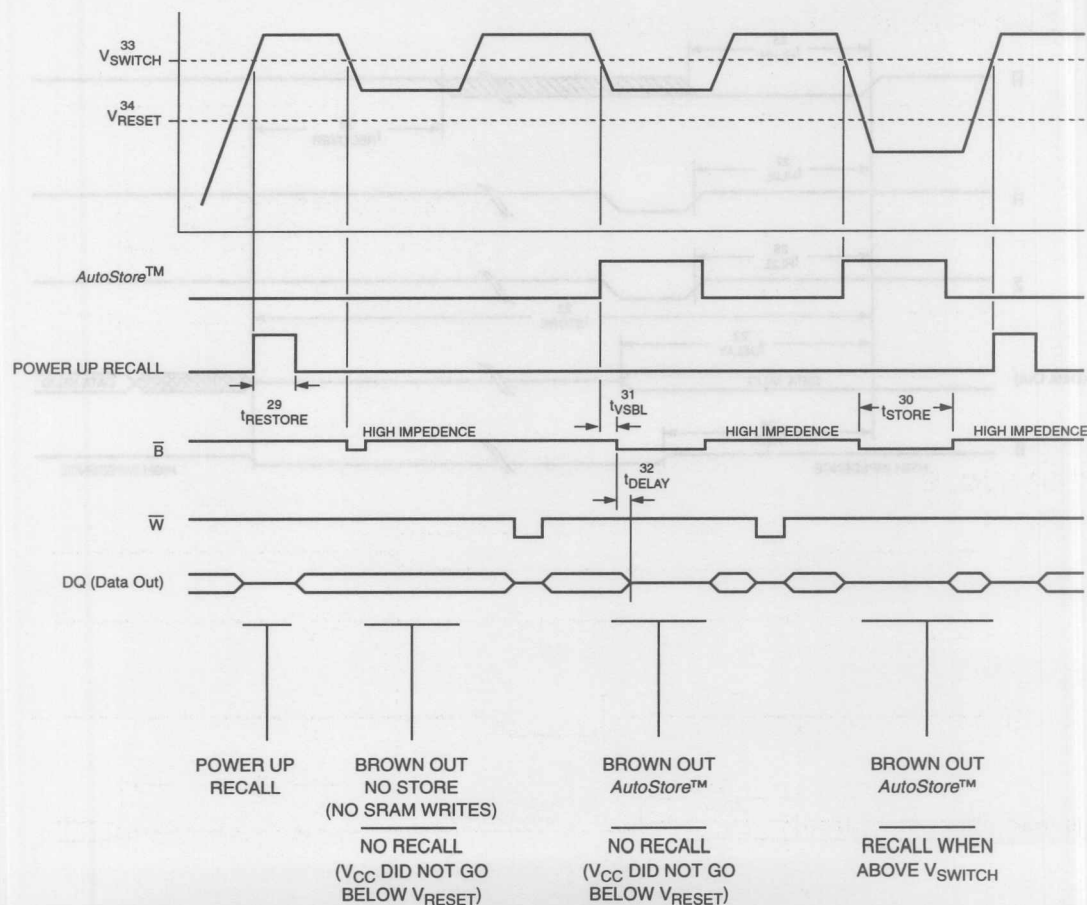


AutoStore™ / POWER UP RECALL
 $(V_{CCX} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK12C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
29	$t_{RESTORE}$		Power Up RECALL Duration		550	μs	t
30	t_{STORE}	t_{BLBZ}	STORE Cycle Duration		10	ms	n, q, u
31	t_{VSB}		Low Voltage Trigger (V_{SWITCH}) to Busy Low		300	ns	k
32	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		μs	n, q
33	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
34	V_{RESET}		Low Voltage Reset Level		3.6	V	

Note t: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH} .

Note u: $\bar{B}$ is asserted low for 1 μs when discharging through V_{SWITCH} . If an SRAM Write has not taken place since the last nonvolatile cycle, $\bar{B}$ will be released and no STORE will take place.

AutoStore™ / POWER UP RECALL


HARDWARE RESET/RECALL & SLEEP CYCLES

($V_{CCX} = 5.0V \pm 10\%$)

NO.	SYMBOLS	PARAMETER	STK12C88		UNITS	NOTES
			MIN	MAX		
35	t_{RLRH}	Reset Enable Pulse Width	20		ns	
36	t_{RLHL}	Reset Enable Set-up Time	0		ns	
37	t_{RLQV}	Reset Cycle Duration		550	μs	q
38	t_{RHQV}	Reset Disable to Data Valid		50	ns	q, y
39	t_{RLQZ}	Reset Enable to Output Inactive		100	ns	n, w
40	t_{ZLZH}	Sleep Enable Pulse Width	20		ns	v
41	t_{ZLQZ}	Sleep Enable to Output Inactive		300	ns	n, x
42	t_{ZLHL}	Sleep Enable Set-up Time	10		ns	
43	t_{ZHQV}	Sleep Disable High to Output Valid		550	μs	q

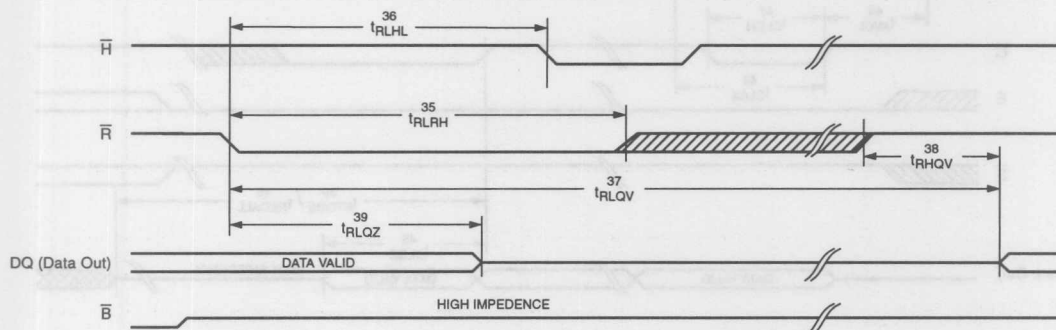
Note v: Sleep current, I_{ZZ} , only occurs while $\bar{Z} \leq 0.2V$ and $\bar{R} \geq (V_{CCX} - 0.2V)$ after t_{ZLQZ} .

Note w: $\bar{E}$ and $\bar{G}$ low and S, $\bar{Z}$ and H high for output behavior.

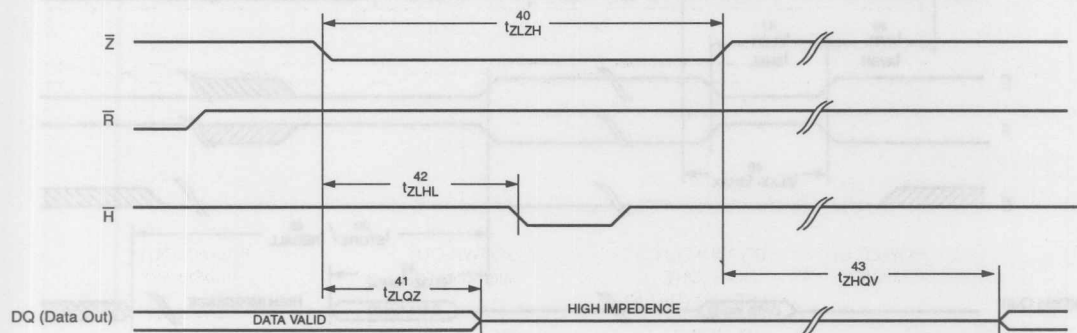
Note x: $\bar{E}$ and $\bar{G}$ low and S, R and H high for output behavior.

Note y: t_{RHQV} is only applicable once t_{RLQV} has been satisfied.

HARDWARE RESET/RECALL CYCLE



SLEEP CYCLE

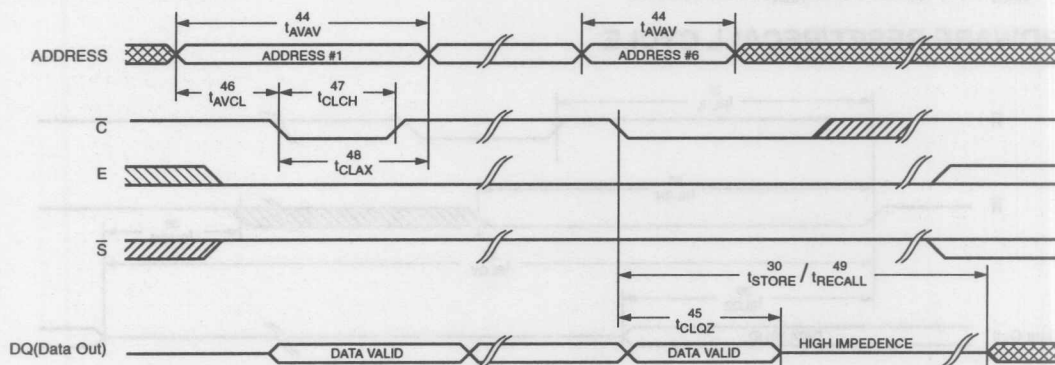
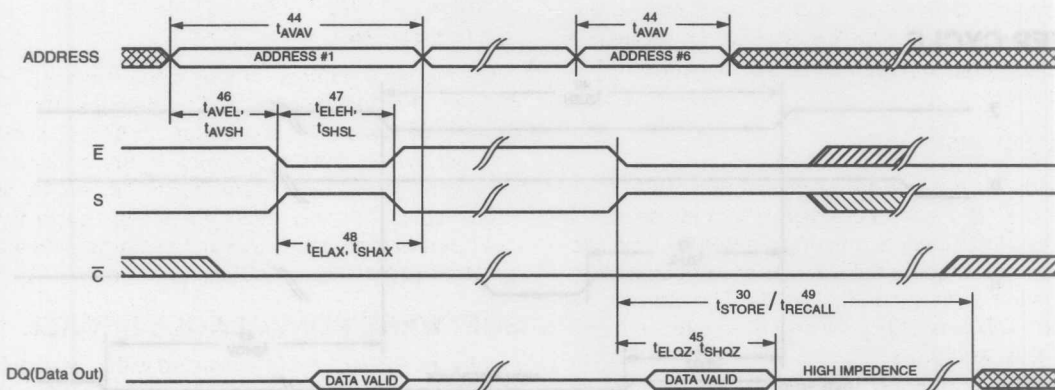


SOFTWARE CYCLES #1 & #2^{aa}
 $(V_{CCX} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK12C88-25		STK12C88-35		STK12C88-45		UNITS	NOTES
	#1	#2		MIN	MAX	MIN	MAX	MIN	MAX		
44	t_{AVAV}		STORE/RECALL Initiation Cycle Time	25		35		45		ns	x
45	t_{CLOZ}	t_{SHOZ}	End of Sequence to Outputs Inactive		600		600		600	ns	q, z
46	t_{AVCL}	t_{AVEL} , t_{AVSH}	Address Set-up Time	0		0		0		ns	z
47	t_{CLCH}	t_{ELEH} , t_{SHSL}	Clock Pulse Width	20		25		30		ns	z
48	t_{CLAX}	t_{ELAX} , t_{SHAX}	Address Hold Time	15		15		15		ns	z
49	t_{RECALL}		Recall Duration		20		20		20	μs	

Note z: The software sequence is clocked with $\bar{E}$ or S controlled reads assuming $\bar{C}$ is low, or clocked by $\bar{C}$ if the STK12C88 is already in SRAM read mode. The Boolean definition of the software clock function is $\bar{C} \cdot (\bar{E} \cdot E1) \cdot (S + S1)$.

Note aa: The six consecutive addresses must be in the order listed in the SOFTWARE MODE SELECTION Table - (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a STORE cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a RECALL cycle. $\bar{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE #1: $\bar{C}$ CONTROLLED^{q,aa}

SOFTWARE CYCLE #2: $\bar{E}$ OR S CONTROLLED^{q,aa}


DEVICE OPERATION

The STK12C88 is a versatile memory chip that provides several modes of operation. The STK12C88 can operate as a standard 32K x 8 SRAM. It has a 32K x 8 EEPROM shadow to which the SRAM information can be copied or from which the SRAM cells can be updated. It also offers systems features such as RESET, SLEEP and multiple chip control options. The mode is determined by either the state of the control pins or by execution of software sequences.

NOISE CONSIDERATIONS

The STK12C88 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 μ F connected between DUT V_{CAP} and V_{SS} , using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK12C88 performs a READ cycle whenever $\bar{E}$ and $\bar{G}$ are low and $\bar{W}$, S , $\bar{R}$, $\bar{Z}$ and $\bar{H}$ are high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\bar{E}$, S or $\bar{G}$, the outputs will be valid at t_{ELQV} , t_{SHQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\bar{E}$ or $\bar{G}$ is brought high or S is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\bar{E}$ and $\bar{W}$ are low and S , $\bar{R}$, $\bar{Z}$ and $\bar{H}$ are high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\bar{E}$ or $\bar{W}$ goes high or S goes low at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\bar{W}$ controlled WRITE or t_{DVEH} or t_{DVSL} before the end of an $\bar{E}$ or S , respectively, controlled WRITE.

It is recommended that $\bar{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on

common I/O lines. If $\bar{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\bar{W}$ goes low.

SOFTWARE NONVOLATILE STORE

The STK12C88 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address	0E38 (hex)	Valid READ
2. Read address	31C7 (hex)	Valid READ
3. Read address	03E0 (hex)	Valid READ
4. Read address	3C1F (hex)	Valid READ
5. Read address	303F (hex)	Valid READ
6. Read address	0FC0 (hex)	Initiate STORE cycle

The software sequence can be clocked with $\bar{E}$ or S controlled reads assuming $\bar{C}$ is low, or clocked by $\bar{C}$ if the STK12C88 is already enabled. The Boolean definition of the software clock function is $\bar{C} \cdot (\bar{E} \cdot \bar{E}1) \cdot (S + S1)$.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\bar{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed with the software clock, $\bar{C}$, low:

1. Read address	0E38 (hex)	Valid READ
2. Read address	31C7 (hex)	Valid READ
3. Read address	03E0 (hex)	Valid READ
4. Read address	3C1F (hex)	Valid READ
5. Read address	303F (hex)	Valid READ
6. Read address	0C63 (hex)	Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AutoStore™ OPERATION

During normal operation, the STK12C88 will draw current from V_{CCX} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a STORE operation.

Figure 1 (page 4-2) shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of at least 100 μf ($\pm 20\%$) rated at 6V should be provided for the STK12C88.

If an automatic STORE on power loss is not required then V_{CAP} should be tied directly to the power supply and V_{CCX} should be tied to ground as shown in figure 2 (page 4-2). In this mode, STORE operations may be triggered through software control or the $\bar{H}$ pin. In either event, V_{CAP} must always have a proper bypass capacitor connected to it.

In order to prevent unneeded STORE operations, automatic STOREs as well as those initiated by externally driving $\bar{H}$ low will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place.

POWER UP RECALL

During power up, or after any low power condition ($V_{\text{CAP}} < V_{\text{RESET}}$) an internal recall request will be latched. When V_{CAP} once again exceeds the sense

voltage of V_{SWITCH} , a RECALL cycle will automatically be initiated and will take t_{RESTORE} to complete.

$\bar{H}$ AND $\bar{B}$ OPERATION

The STK12C88 provides the $\bar{H}$ and $\bar{B}$ pins for controlling and acknowledging the STORE operations. The $\bar{H}$ pin is used to request a hardware STORE cycle. When the $\bar{H}$ pin is driven low, the STK12C88 will conditionally initiate a STORE operation after t_{DELAY} : an actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\bar{B}$ pin is an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\bar{H}$ is driven low or after an AutoStore™ cycle is requested and $\bar{B}$ is pulled low, are given time to complete before the STORE operation is initiated. After $\bar{H}$ goes low, the STK12C88 will continue SRAM operations for t_{DELAY} . During t_{DELAY} , multiple SRAM READ operations may take place. If a WRITE is in progress when $\bar{B}$ is pulled low it will be allowed a time, t_{DELAY} , to complete. However, any SRAM WRITE cycles requested after $\bar{B}$ transitions low will be inhibited.

The $\bar{H}$ and $\bar{B}$ pins can be used to synchronize multiple STK12C88s while using a single larger capacitor. To operate in this mode the $\bar{H}$ and $\bar{B}$ pins should be connected together and to the $\bar{H}$ and $\bar{B}$ pins from the other STK12C88s. An external pull up resistor to +5V is needed since $\bar{B}$ is an open drain pull down. Do not connect this or any other pull-up to the V_{CAP} pin. The V_{CAP} pins from the other STK12C88 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK12C88s detects a power loss and asserts $\bar{B}$, the common $\bar{H}$ pin will cause all parts to request a STORE cycle (a STORE will take place in those STK12C88s that have been written since the last nonvolatile cycle).

During any STORE operation, regardless of how it was initiated, the STK12C88 will continue to drive the $\bar{B}$ pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the STK12C88 will remain disabled until the $\bar{H}$ pin is brought high.

HARDWARE RESET

A hardware RESET cycle is performed when $\bar{R}$ is brought low, interrupting any cycle in progress with the exception of STORE cycles (assuming t_{HLRL} has been satisfied). $\bar{R}$ interfaces directly to the system reset. RESET, which includes an internally-generated RECALL cycle, takes t_{RLQV} to complete as long as $V_{CAP} > V_{SWITCH}$. If $\bar{R}$ is kept low after the RESET is completed all other pins will remain disabled and the current consumption will be I_{SB2} . Bringing $\bar{R}$ high after the RESET has finished (i.e. $t > t_{RLQV}$) enables the SRAM quickly, within only t_{RHQV} .

Control clock priority is, from highest to lowest: $\bar{R}$; $\bar{Z}$; $\bar{H}$; SRAM control pins. For example, if the $\bar{Z}$ and $\bar{H}$ pins are asserted in unison the part will go to SLEEP rather than STORE.

HARDWARE PROTECT

The STK12C88 offers hardware protection against inadvertent STORE operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$ all externally initiated STORE operations will be inhibited.

AutoStore™ can be completely disabled by tying V_{CCX} to ground and applying +5V to V_{CAP} as illustrated in Figure 2. This is the data protect mode; STOREs are only initiated by explicit request using either the software sequence or the $\bar{H}$ pin.

SLEEP MODE

SLEEP mode is initiated by asserting $\bar{Z}$ low. Internally all current loads, including the SRAM array are turned off, reducing current consumption to near zero. This will, of course, cause all SRAM data to be lost. A STORE must be explicitly requested by the user t_{HLZL} before asserting $\bar{Z}$ if the SRAM data is to be preserved. Note that *AutoStore™* and all other operations with the exception of RESET are disabled when $\bar{Z}$ is low. On the rising edge of $\bar{Z}$ a POWER UP RECALL cycle is initiated lasting t_{ZHQV} so long as $V_{CAP} > V_{SWITCH}$.

LOW AVERAGE ACTIVE POWER

The STK12C88 will draw significantly less current when it is cycled at times longer than 30ns. Figure 5, below, shows the relationship between I_{CC} and READ cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, $V_{CC} = 5.5V$, 100% duty cycle on chip enable). Figure 6 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled.

The overall average current drawn by the STK12C88 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READ's to WRITE's; 5) the operating temperature; 6) the V_{CCX} level and; 7) I/O loading.

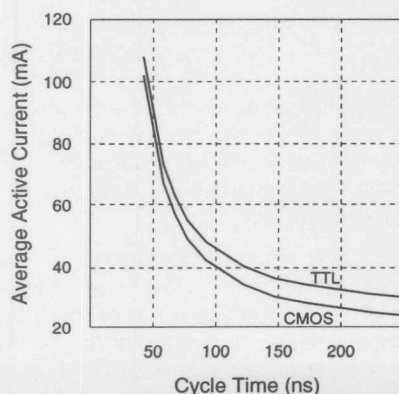


Fig 5: I_{CC} (max) Reads

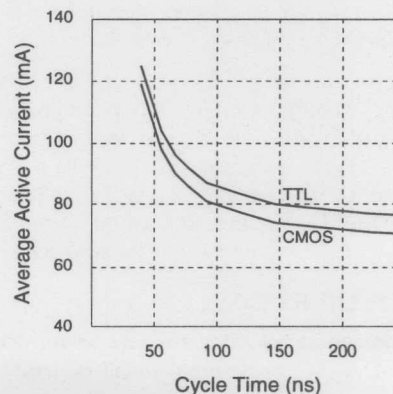


Fig 6: I_{CC} (Max) Writes

ORDERING INFORMATION

STK12C88 - Q 35 I

Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

Q = Plastic Quad Flat Pack

W = Plastic 40-pin 600 mil PDIP



STK12C816

16K x 16 *AutoStore*™ nvSRAM

High Performance CMOS

Nonvolatile Static RAM

PRELIMINARY

FEATURES

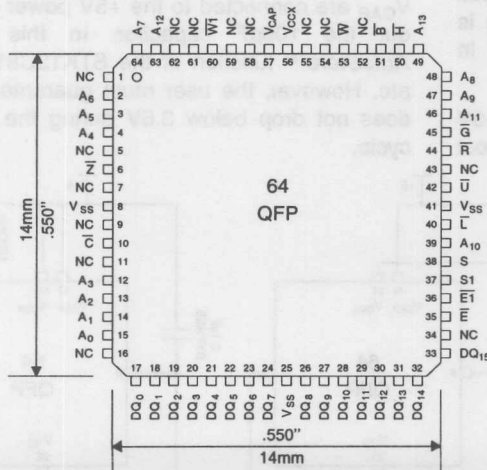
- 25ns, 35ns and 45ns Access Times
- 16 Bit Wide I/O Path for DSP Interface
- Store to EEPROM Initiated by Hardware, Software or *AutoStore*™ on Power Down
- Recall to SRAM Initiated by Hardware Reset, Software or Power Restore
- "Hands-off" Store with 100μF Capacitor
- Low Power Sleep Mode: $I_{CC} < 10\mu A$
- 25mA I_{CC} at 200ns Cycle Time
- Multiple Select and Enable Pins for Flexible Interface to Processors
- Separate Strobe Input for Software Control
- Unlimited Recalls from EEPROM to SRAM
- 100,000 Store Cycles to EEPROM
- 10 Year Data Retention in EEPROM
- Commercial and Industrial Temp. Ranges
- 64 Pin PQFP Package

DESCRIPTION

The Simtek STK12C816 is a fast static RAM with a nonvolatile, electrically-erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down using charge stored in an external capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of STORE and RECALL cycles can also be controlled by separate input pins or by entering control sequences on the SRAM inputs. Hardware reset and low power SLEEP mode functions are included.

5

PACKAGE DIAGRAM

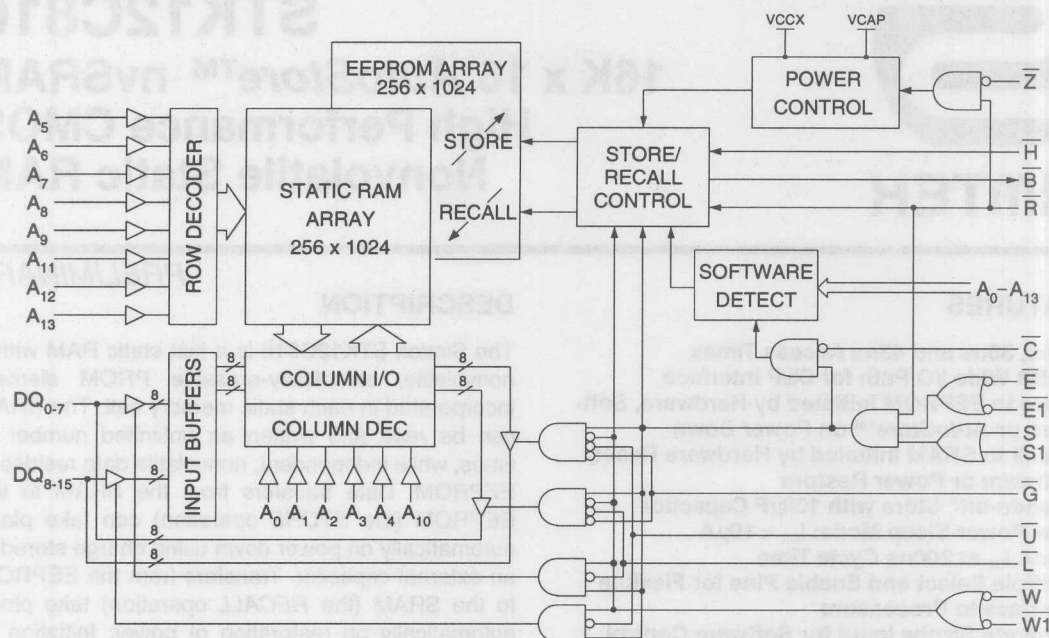


PIN NAMES

A ₀ - A ₁₃	Address Inputs
DQ ₀ - DQ ₁₅	Data In/Out
$\bar{E}$, $\bar{E}1$	Chip Enables (Low)
S, S1	Chip Selects (High)
$\bar{W}$, $\bar{W}1$	Write Enables
$\bar{G}$	Output Enable
$\bar{U}$	Upper Byte Select
$\bar{L}$	Lower Byte Select
$\bar{H}$	Hardware Store
$\bar{R}$	Hardware Reset
$\bar{B}$	Store Busy
$\bar{C}$	Software Clock
$\bar{Z}$	Sleep Mode Enable
V _{CCX}	Power (+5V)
V _{CAP}	Capacitor
V _{SS}	Ground

STK12C816

BLOCK DIAGRAM



POWER SUPPLY CONNECTION OPTIONS

The STK12C816 can be powered in three modes. In the normal mode, 5V is supplied to V_{CCX} and a 100μF capacitor is connected to the V_{CAP} terminal, as shown in Figure 1. This datasheet is written assuming that this configuration is used so power supply specifications will refer to V_{CCX}. An optional pull up resistor is shown connected to B-bar. This is used to signal that the *AutoStore*[™] cycle is in progress.

Optionally, V_{CCX} can be tied to ground and +5V applied to V_{CAP} (Figure 2). This is the data protect

mode in which the *AutoStore*[™] function is disabled. If the STK12C816 is operated in this configuration, references to V_{CCX} should be changed to V_{CAP} throughout this data sheet.

In system power mode (Figure 3) both V_{CCX} and V_{CAP} are connected to the +5V power supply without the 100μF capacitor. In this mode the *AutoStore*[™] function of the STK12C816 will operate. However, the user must guarantee that V_{CCX} does not drop below 3.6V during the 10ms store cycle.

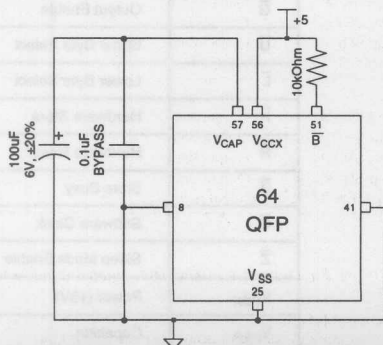


Figure 1: *AutoStore*[™] Mode

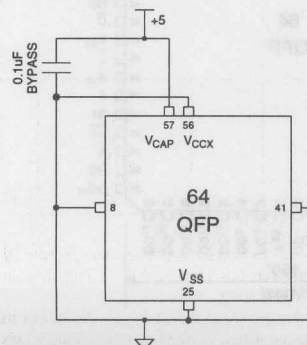


Figure 2: Data Protect Mode

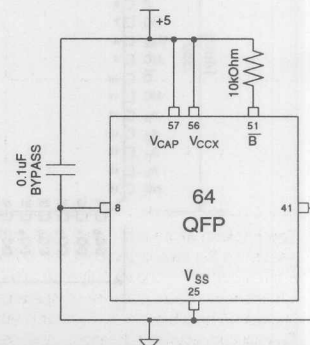


Figure 3: System Power Mode

MULTIPLE CONTROL INPUTS

The STK12C816 provides dual control pins for each of the primary SRAM control functions, chip enable ($\overline{E}$), chip select (S) and write enable ($\overline{W}$). The secondary input carries the suffix "1", e.g. $\overline{E}1$. These multiple inputs are provided for ease of interface to various processors and control chips. They allow such functions as data and program access to the same STK12C816 chip and independent control of the nonvolatile software sequences.

Either control pin from each pair may be used interchangeably. For the sake of brevity, this datasheet references only the non-suffix input per pair but all AC and DC specifications apply to both.

Logical AND and OR chip selection is possible using

the chip select and chip enable input pairs. To select the chip, S or S1 must be active HIGH and $\overline{E}$ or $\overline{E}1$ must be active LOW. The Boolean definition is $(\overline{E} \cdot \overline{E}1) \cdot (S + S1)$. The SRAM write function is enabled when $\overline{W}$ or $\overline{W}1$ is active low.

An additional input, $\overline{C}$, is provided for more flexible control of the software modes (see software mode selection table). The software sequence can be clocked with $\overline{E}$ or S controlled reads assuming $\overline{C}$ is low, or clocked by $\overline{C}$ if the STK12C816 is already enabled. The Boolean definition of the software clock function is $\overline{C} \cdot (\overline{E} \cdot \overline{E}1) \cdot (S + S1)$. If the additional control is not needed the $\overline{C}$ pin can be tied to 0V. The software clock, $\overline{C}$, has no effect on SRAM cycles.

HARDWARE MODE SELECTION

$\overline{E}$	S	$\overline{U}$	$\overline{L}$	$\overline{W}$	$\overline{G}$	$\overline{H}$	$\overline{Z}$	$\overline{R}$	MODE	POWER	NOTES
H	X	X	X	X	X	H	H	H	Not selected	Standby	a
X	L	X	X	X	X	H	H	H	Not selected	Standby	a
L	H	L	L	H	L	H	H	H	Read RAM (x16 word)	Active	
L	H	L	L	H	L	H	H	H	Write RAM (x16 word)	Active	b
L	H	L	H	H/L	L	H	H	H	Read/Write Upper Byte	Active	b
L	H	H	L	H/L	X	H	H	H	Read/Write Lower Byte	Active	b
X	X	X	X	X	X	L	X	X	Nonvolatile STORE	I_{CC2}	c, d
X	X	X	X	X	X	X	L	H	SLEEP mode	I_{ZZ}	
X	X	X	X	X	X	X	X	L	Hardware RESET / RECALL	Standby	

SOFTWARE MODE SELECTION

$\overline{E}$	S	$\overline{C}$	$\overline{W}$	$\overline{R}$	$\overline{H}$	$\overline{Z}$	A ₁₃ - A ₀ (hex)	MODE	I/O	NOTES
L	H	H	H	H	H	H	X	Read SRAM Software Disabled	Output data	
L	H	L	H	H	H	H	0E38 31C7 03E0 3C1F 303F 0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output data Output data Output data Output data Output data Output high Z	e
L	H	L	H	H	H	H	0E38 31C7 03E0 3C1F 303F 0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output data Output data Output data Output data Output data Output high Z	e

Note a: The Boolean expression of chip selection is $(\overline{E} \cdot \overline{E}1) \cdot (S + S1)$.

Note b: Assuming the chip is selected, the Boolean expression for write selection is $(\overline{W} \cdot \overline{W}1)$.

Note c: $\overline{H}$ store operation occurs only if an SRAM write has been done since the last nonvolatile cycle. After the store (if any) completes the part will go into standby mode inhibiting all operations until $\overline{H}$ rises.

Note d: $\overline{R}$ must be held high for t_{HLRL} after $\overline{H}$ otherwise the store cycle may be aborted by the reset request.

Note e: The six consecutive addresses must be in order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

STK12C816

ABSOLUTE MAXIMUM RATINGS^f

Voltage on input relative to V_{SS} -0.5V to ($V_{CCX} + 0.5V$)
 Voltage on DQ_{0-15} or $\bar{B}$ -0.5V to ($V_{CCX} + 0.5V$)
 Temperature under bias -55°C to 125°C
 Storage temperature -65°C to 150°C
 Power dissipation 1W
 DC output current (1 output at a time, 1s duration) 15mA

Note f: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CCX} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^g	Average V_{CCX} Current		155 135 115		170 150 130	mA	$t_{AVAV} = 25ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$
I_{CC2}^h	Average V_{CCX} Current During STORE		6		7	mA	All inputs Don't Care
I_{CC3}^g	Average V_{CCX} Current at $t_{AVAV} = 200ns$		25		25	mA	$\bar{W} \geq (V_{CCX} - 0.2V)$ All others cycling, CMOS levels
I_{CC4}^h	Average V_{CAP} Current During <i>AutoStore</i> TM Cycle		4		4	mA	All inputs Don't Care
I_{SB1}^i	Average V_{CCX} Current (Standby, Cycling TTL Input Levels)		40 36 33		42 38 35	mA	$t_{AVAV} = 25ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 35ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 45ns, \bar{E} \geq V_{IH}$
I_{SB2}^i	V_{CCX} Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\bar{E} \geq (V_{CCX} - 0.2V)$ or $S \leq 0.2V$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CCX} - 0.2V)$
I_{ZZ}	V_{CCX} Current During Sleep Mode		10		10	μA	$\bar{Z} \leq 0.2V; \bar{R} \geq (V_{CCX} - 0.2V)$; all others Don't Care. Typical current = 2 μA
I_{ILK}	Input Leakage Current		± 1		± 1	μA	$V_{CCX} = \max$ $V_{IN} = V_{SS}$ to V_{CCX}
I_{OLK}	Off-State Output Leakage Current		± 1		± 1	μA	$V_{CCX} = \max$ $V_{IN} = V_{SS}$ to V_{CCX} , $\bar{E}$ or $\bar{G} \geq V_{IH}$ or $S \leq V_{IL}$
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CCX} + .5$	2.2	$V_{CCX} + .5$	V	All inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS} - .5$	0.8	$V_{SS} - .5$	0.8	V	All inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
V_{BL}	Logic "0" Voltage on $\bar{B}$ Output		0.4		0.4	V	$I_{OUT} = 3mA$
T_A	Operating Temperature	0	70	-40	85	°C	

Note g: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note h: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).

Note i: $\bar{E} \geq V_{IH}$ or $S \leq V_{IL}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input pulse levels 0V to 3V
 Input rise and fall times $\leq 5ns$
 Input and output timing reference levels 1.5V
 Output load See Figure 4

CAPACITANCE^j ($T_A = 25^\circ C, f = 1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output capacitance	7	pF	$\Delta V = 0$ to 3V

Note j: These parameters are guaranteed but not tested.

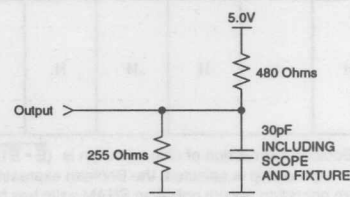


Figure 4: AC Output Loading

SRAM READ CYCLES #1 & #2ⁿ
 $(V_{CCX} = 5.0V \pm 10\%)$

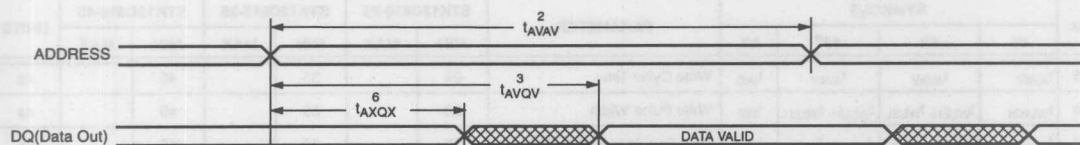
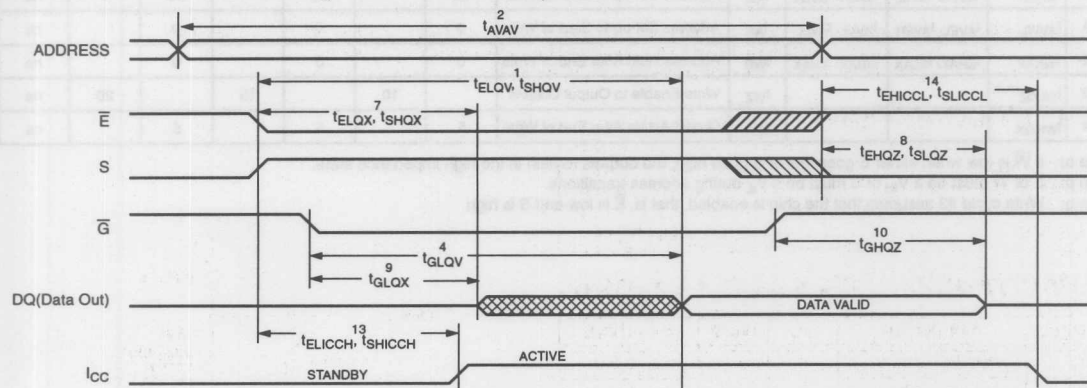
NO.	SYMBOLS		PARAMETER	STK12C816-25		STK12C816-35		STK12C816-45		UNITS
	#1, #2, #3	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}^1, t_{SHQV}^1	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}^k	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}^l	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{ULQV}, t_{LLQV}	t_{AB}	Byte select to data valid		10		15		20	ns
6	t_{AXQX}^l	t_{OH}	Output Hold After Address Change	3		3		3		ns
7	t_{ELQX}, t_{SHQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
8	t_{EHQZ}, t_{SLQZ}^m	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
9	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
10	t_{GHQZ}^m	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
11	t_{ULQX}, t_{LLQX}	t_{BLZ}	Byte select to output active	0		0		0		ns
12	t_{UHQZ}, t_{LHQZ}^m	t_{BHZ}	Byte select to output inactive		10		15		20	ns
13	t_{ELICCH}, t_{SHICCH}^l	t_{PA}	Chip Enable to Power Active	0		0		0		ns
14	$t_{EHICCL}, t_{SLICCL}^{l,i}$	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

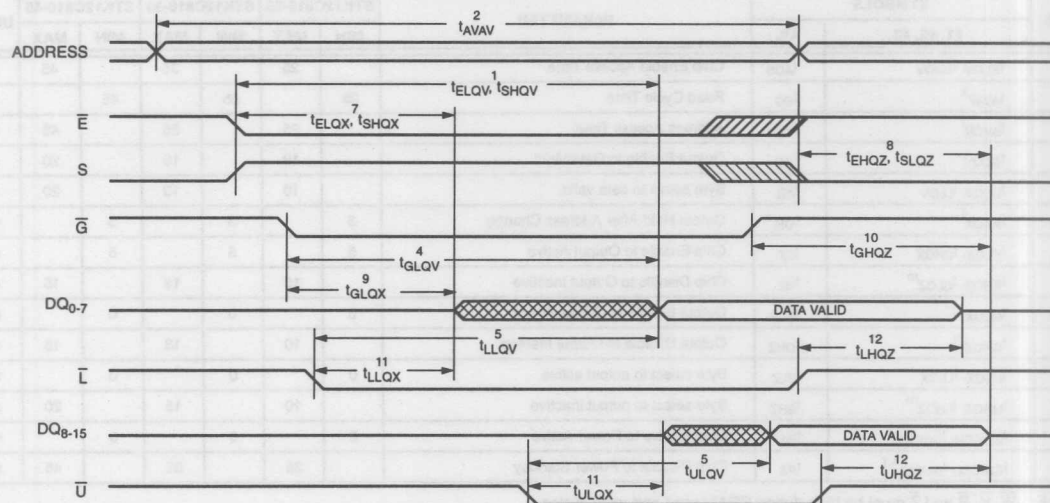
Note k: $\bar{W}$, $\bar{H}$, $\bar{R}$ and $\bar{Z}$ must be high during SRAM read and write cycles.

Note l: Device is continuously selected with $\bar{E}$ and $\bar{G}$ both low, at least one of $\bar{U}$ or $\bar{L}$ low, and S high.

Note m: Measured $\pm 200mV$ from steady state output voltage

Note n: One or both of $\bar{U}$ or $\bar{L}$ must be low for SRAM access

SRAM READ CYCLE #1 (Address Controlled)^{k, l, n}

SRAM READ CYCLE #2 ($\bar{E}$ or S controlled)^{k, n}


SRAM READ CYCLE #3 ($\bar{U}$ or $\bar{L}$ controlled)

SRAM WRITE CYCLES #1, #2 & #3ⁿ
 $(V_{CCX} = 5.0V \pm 10\%)$

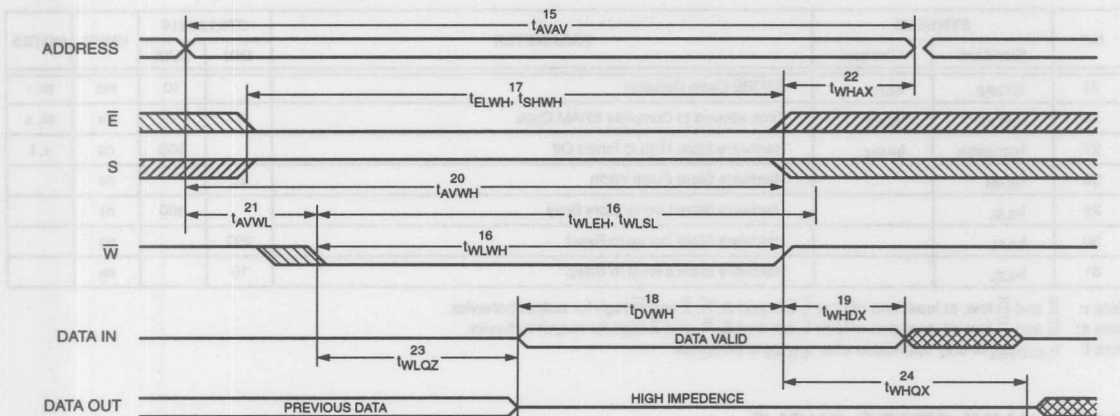
NO.	SYMBOLS				PARAMETER	STK12C816-25		STK12C816-35		STK12C816-45		UNITS
	#1	#2	#3 ^q	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
15	t_{AVAV}	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
16	t_{WLWH}	t_{WLEH}, t_{WLSL}	t_{WLUH}, t_{WLLH}	t_{WP}	Write Pulse Width	20		30		40		ns
17	t_{ELWH}	t_{ELEH}, t_{SHSL}	t_{ULUH}, t_{ULLH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns
18	t_{DVWH}	t_{DVEH}, t_{DVSL}	t_{DVUH}, t_{DVLH}	t_{DW}	Data Set-up to End of Write	10		13		17		ns
19	t_{WHDX}	t_{EHDX}, t_{SLDX}	t_{UHDX}, t_{LHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
20	t_{AVWH}	t_{AVEH}, t_{AVSL}	t_{AVUH}, t_{AVLH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns
21	t_{AVWL}	t_{AVEL}, t_{AVSH}	t_{AVUL}, t_{AVLL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
22	t_{WHAX}	t_{EHAX}, t_{SLAX}	t_{UHAX}, t_{LHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
23	$t_{WLOZ}^{m,o}$			t_{WZ}	Write Enable to Output Disable		10		15		20	ns
24	t_{WHQX}			t_{OW}	Output Active After End of Write	5		5		5		ns

Note o: If $\bar{W}$ is low when either $\bar{E}$ goes low or S goes high, the outputs remain in the high impedance state.

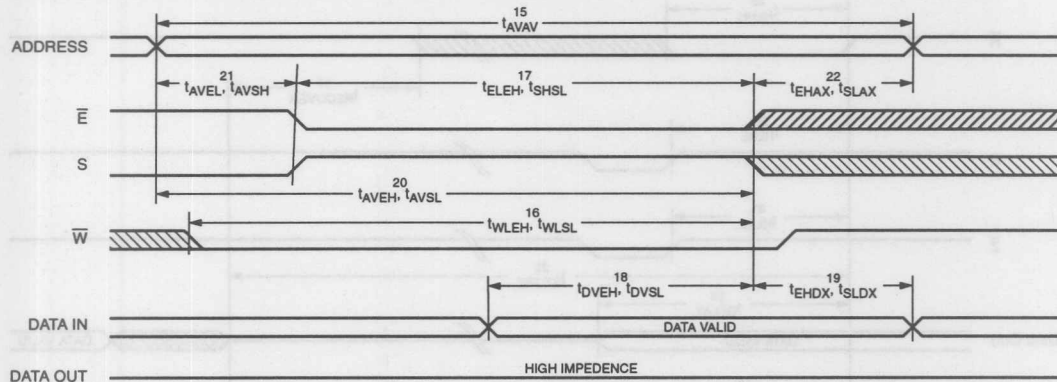
Note p: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ or S must be $\leq V_{IL}$ during address transitions.

Note q: Write cycle #3 assumes that the chip is enabled, that is, $\bar{E}$ is low and S is high

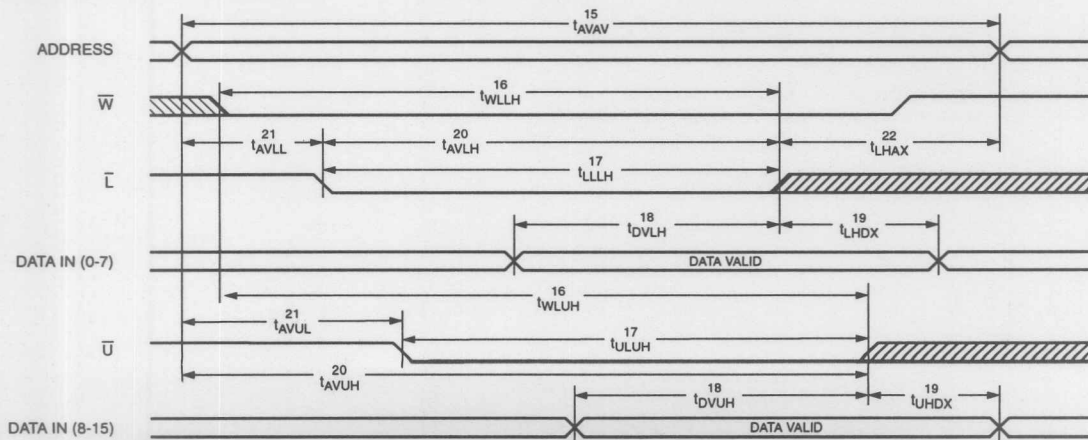
SRAM WRITE CYCLE #1: $\overline{W}$ CONTROLLED^{p, k}



SRAM WRITE CYCLE #2: $\overline{E}, \overline{S}$ CONTROLLED^{p, k}



SRAM WRITE CYCLE #3: $\overline{U}, \overline{L}$ CONTROLLED^q



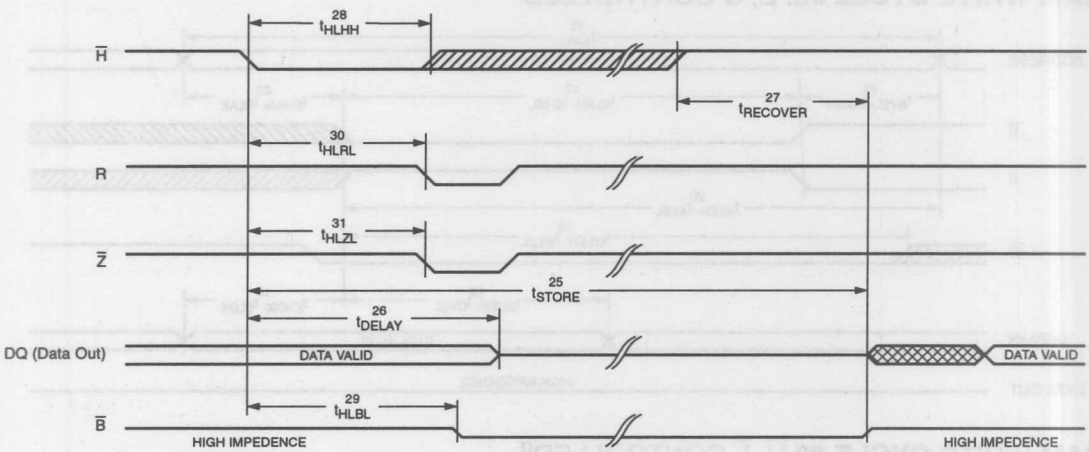
HARDWARE STORE CYCLE

(V_{CCX} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK12C816		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
25	t _{STORE}	t _{HLBZ}	STORE Cycle Duration		10	ms	m, r
26	t _{DELAY}	t _{HLOZ}	Time allowed to Complete SRAM Cycle	1		μs	m, s
27	t _{RECOVER}	t _{HHQX}	Hardware Store High to Inhibit Off		200	ns	r, t
28	t _{HLHH}		Hardware Store Pulse Width	20		ns	
29	t _{HLBL}		Hardware Store Low to Store Busy		300	ns	
30	t _{HLRL}		Hardware Store Set-up to Reset	300		ns	
31	t _{HLZL}		Hardware Store Set-up to Sleep	10		ns	

Note r: $\overline{E}$ and $\overline{G}$ low, at least one of $\overline{U}$ or $\overline{L}$ low and S, $\overline{R}$, $\overline{Z}$ and $\overline{H}$ high for output behavior.
Note s: $\overline{E}$ and $\overline{G}$ low, at least one of $\overline{U}$ or $\overline{L}$ low and S, R, and $\overline{Z}$ high for output behavior.
Note t: t_{RECOVER} is only applicable after t_{STORE} is complete.

HARDWARE STORE CYCLE



AutoStore™ / POWER UP RECALL

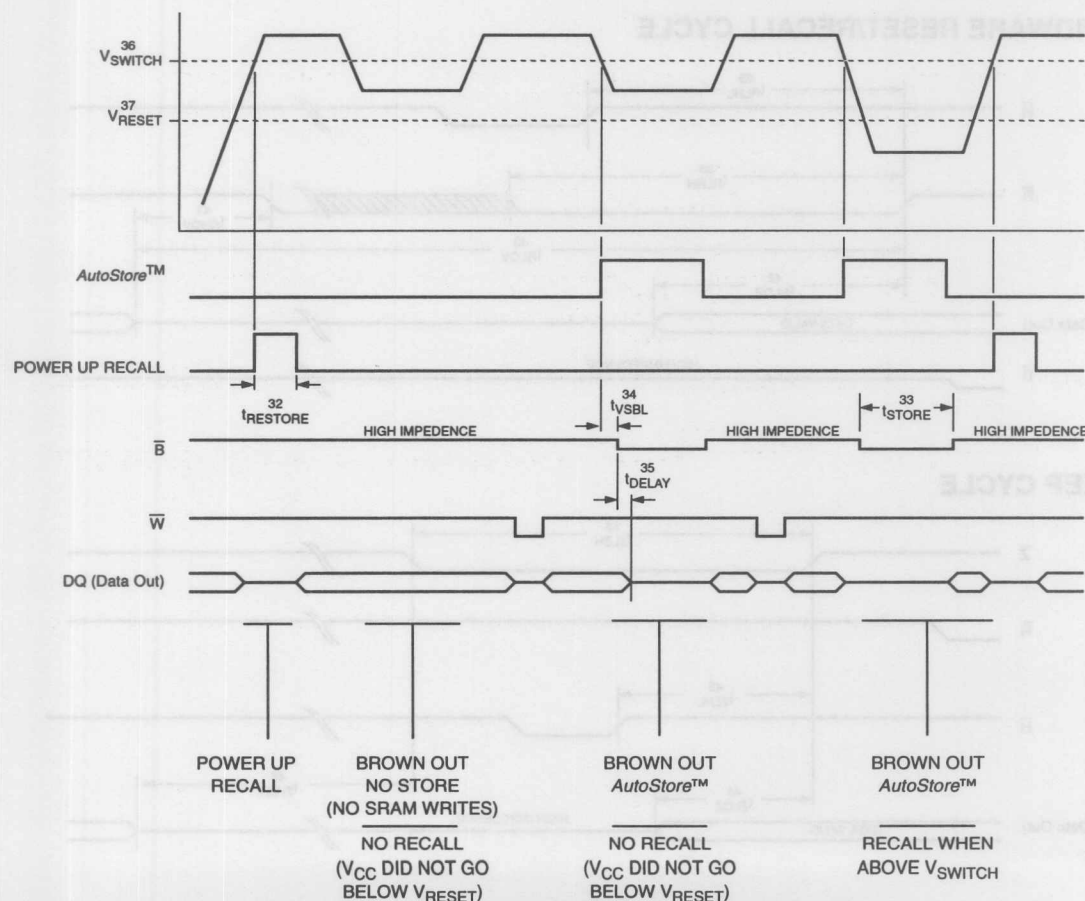
(V_{CCX} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK12C816		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
32	t _{RESTORE}		Power Up RECALL Duration		550	μs	u
33	t _{STORE}	t _{BLBZ}	STORE Cycle Duration		10	ms	n, r, v
34	t _{VSBL}		Low Voltage Trigger (V _{SWITCH}) to Busy Low		300	ns	j
35	t _{DELAY}	t _{BLQZ}	Time Allowed to Complete SRAM Cycle	1		μs	n, r
36	V _{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
37	V _{RESET}		Low Voltage Reset Level		3.6	V	

Note u: t_{RESTORE} starts from the time V_{CC} rises above V_{SWITCH}.

Note v: $\bar{B}$ is asserted low for 1μs when discharging through V_{SWITCH}. If an SRAM Write has not taken place since the last nonvolatile cycle, $\bar{B}$ will be released and no STORE will take place.

AutoStore™ / POWER UP RECALL



HARDWARE RESET/RECALL & SLEEP CYCLES
 $(V_{CCX} = 5.0V \pm 10\%)$

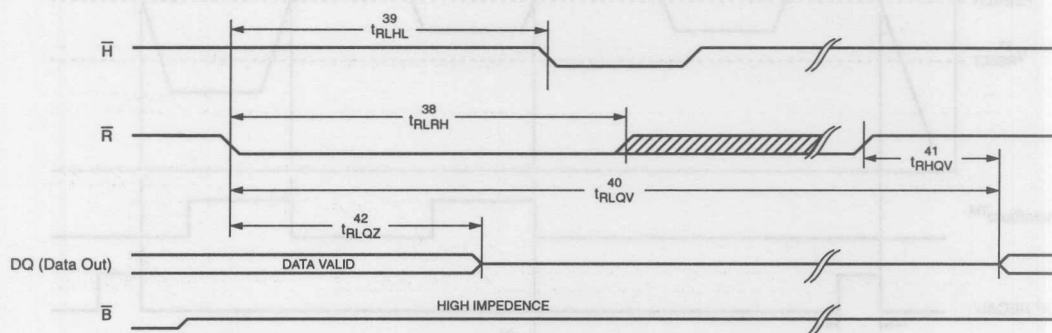
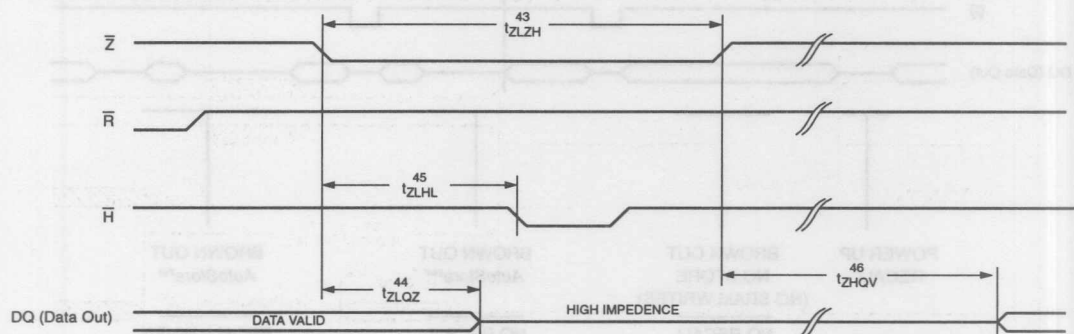
NO.	SYMBOLS	PARAMETER	STK12C816		UNITS	NOTES
			MIN	MAX		
38	t_{RLRH}	Reset Enable Pulse Width	20		ns	
39	t_{RLHL}	Reset Enable Set-up Time	0		ns	
40	t_{RLQV}	Reset Cycle Duration		550	μs	r
41	t_{RHQV}	Reset Disable to Data Valid		50	ns	r, z
42	t_{RLQZ}	Reset Enable to Output Inactive		100	ns	m, x
43	t_{ZLZH}	Sleep Enable Pulse Width	20		ns	w
44	t_{ZLQZ}	Sleep Enable to Output Inactive		300	ns	m, y
45	t_{ZLHL}	Sleep Enable Set-up Time	10		ns	
46	t_{ZHQV}	Sleep Disable High to Output Valid		550	μs	r

Note w: Sleep current, I_{ZZ} , only occurs while $\bar{Z} \leq 0.2V$ and $\bar{R} \geq (V_{CCX} - 0.2V)$ after t_{ZLQZ} .

Note x: $\bar{E}$ and $\bar{G}$ low, at least one of $\bar{U}$ or $\bar{L}$ low and S, Z and H high for output behavior.

Note y: $\bar{E}$ and $\bar{G}$ low, at least one of $\bar{U}$ or $\bar{L}$ low and S, R and H high for output behavior.

Note z: t_{RHQV} is only applicable once t_{RLQV} has been satisfied.

HARDWARE RESET/RECALL CYCLE

SLEEP CYCLE


SOFTWARE CYCLES #1 & #2^{ab}

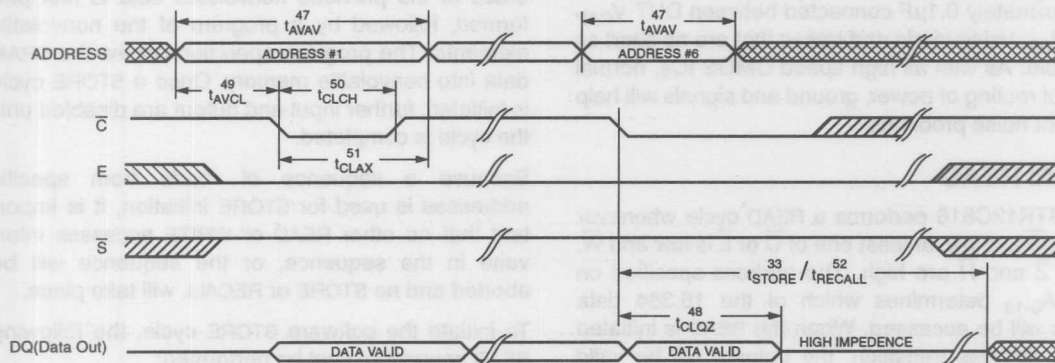
(V_{CCX} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK12C816-25		STK12C816-35		STK12C816-45		UNITS	NOTES
	#1	#2		MIN	MAX	MIN	MAX	MIN	MAX		
47	t _{AVAV}		STORE/RECALL Initiation Cycle Time	25		35		45		ns	y
48	t _{CLOZ}	t _{ELQZ} , t _{SHQZ}	End of Sequence to Outputs Inactive		600		600		600	ns	r aa
49	t _{AVCL}	t _{AVEL} , t _{AVSH}	Address Set-up Time	0		0		0		ns	aa
50	t _{CLCH}	t _{ELEH} , t _{SHSL}	Clock Pulse Width	20		25		30		ns	aa
51	t _{CLAX}	t _{ELAX} , t _{SHAX}	Address Hold Time	15		15		15		ns	aa
52	t _{RECALL}		Recall Duration		20		20		20	μs	

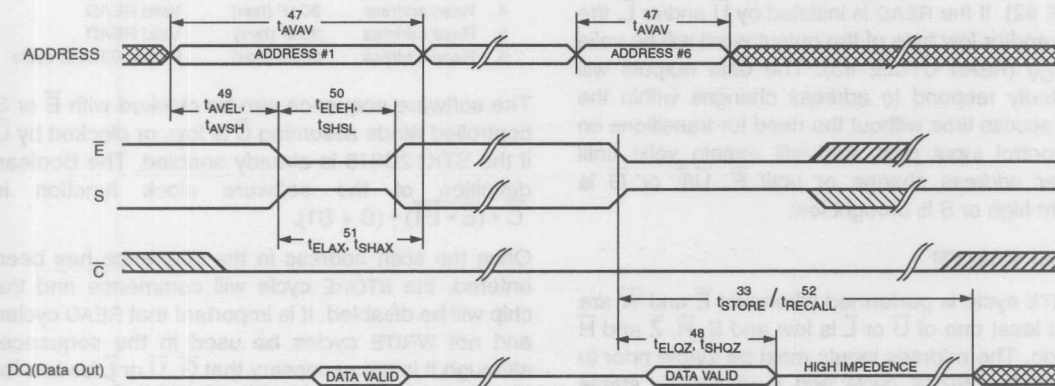
Note aa: The software sequence is clocked with $\bar{E}$ or $\bar{S}$ controlled reads assuming $\bar{C}$ is low, or clocked by $\bar{C}$ if the STK12C816 is already in SRAM read mode. The Boolean definition of the software clock function is $\bar{C} \cdot (\bar{E} \cdot \bar{E}1) \cdot (\bar{S} + \bar{S}1)$.

Note ab: The six consecutive addresses must be in the order listed in the SOFTWARE MODE SELECTION Table - (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a STORE cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a RECALL cycle. $\bar{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE #1: $\bar{C}$ CONTROLLED^{r,ab}



SOFTWARE CYCLE #2: $\bar{E}$ OR $\bar{S}$ CONTROLLED^{r,ab}



DEVICE OPERATION

The STK12C816 is a versatile memory chip that provides several modes of operation. The STK12C816 can operate as a standard 16K x 16 SRAM. It has a 16K x 16 EEPROM shadow to which the SRAM information can be copied or from which the SRAM cells can be updated. It also offers systems features such as RESET, SLEEP and multiple chip control options. The mode is determined by either the state of the control pins or by execution of software sequences.

NOISE CONSIDERATIONS

The STK12C816 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 μ F connected between DUT V_{CAP} and V_{SS} , using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK12C816 performs a READ cycle whenever $\bar{E}$ and $\bar{G}$ are low, at least one of $\bar{U}$ or $\bar{L}$ is low and $\bar{W}$, S , $\bar{R}$, $\bar{Z}$ and $\bar{H}$ are high. The address specified on pins A_{0-13} determines which of the 16,384 data words will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\bar{E}$, S or $\bar{G}$, the outputs will be valid at t_{ELQV} , t_{SHQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). If the READ is initiated by $\bar{U}$ and/or $\bar{L}$, the upper and/or low byte of the output word will be valid at t_{ULQV} (READ CYCLE #3). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\bar{E}$, $\bar{U}/\bar{L}$ or $\bar{G}$ is brought high or S is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\bar{E}$ and $\bar{W}$ are low, at least one of $\bar{U}$ or $\bar{L}$ is low and S , $\bar{R}$, $\bar{Z}$ and $\bar{H}$ are high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\bar{E}$, $\bar{U}/\bar{L}$ or $\bar{W}$ goes high or S goes low at the end of the cycle. The data on the common I/O pins DQ_{0-15} will be written into the memory if it is valid t_{DVWH} before the end of a $\bar{W}$ controlled WRITE

or t_{DVEH} or t_{DVSL} before the end of an $\bar{E}$ or S , respectively, controlled WRITE. If $\bar{U}$ or $\bar{L}$ are used to control the WRITE cycle only the selected portion(s) of the 16 bit word will be written.

It is recommended that $\bar{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\bar{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\bar{W}$ goes low.

SOFTWARE NONVOLATILE STORE

The STK12C816 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address	0E38 (hex)	Valid READ
2. Read address	31C7 (hex)	Valid READ
3. Read address	03E0 (hex)	Valid READ
4. Read address	3C1F (hex)	Valid READ
5. Read address	303F (hex)	Valid READ
6. Read address	0FC0 (hex)	Initiate STORE cycle

The software sequence can be clocked with $\bar{E}$ or S controlled reads assuming $\bar{C}$ is low, or clocked by $\bar{C}$ if the STK12C816 is already enabled. The Boolean definition of the software clock function is $\bar{C} \cdot (\bar{E} \cdot E1) \cdot (S + S1)$.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\bar{G}$, $\bar{U}$ or $\bar{L}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed with the software clock, $\bar{C}$, low:

1. Read address	0E38 (hex)	Valid READ
2. Read address	31C7 (hex)	Valid READ
3. Read address	03E0 (hex)	Valid READ
4. Read address	3C1F (hex)	Valid READ
5. Read address	303F (hex)	Valid READ
6. Read address	0C63 (hex)	Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AutoStore™ OPERATION

During normal operation, the STK12C816 will draw current from V_{CCX} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a STORE operation.

Figure 1 (page 4-2) shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of at least 100 μf ($\pm 20\%$) rated at 6V should be provided for the STK12C816.

If an automatic STORE on power loss is not required then V_{CAP} should be tied directly to the power supply and V_{CCX} should be tied to ground as shown in figure 2 (page 4-2). In this mode, STORE operations may be triggered through software control or the $\bar{H}$ pin. In either event, V_{CAP} must always have a proper bypass capacitor connected to it.

In order to prevent unneeded STORE operations, automatic STORES as well as those initiated by externally driving $\bar{H}$ low will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initi-

ated STORE cycles are performed regardless of whether a WRITE operation has taken place.

POWER UP RECALL

During power up, or after any low power condition ($V_{\text{CAP}} < V_{\text{RESET}}$) an internal recall request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH} , a RECALL cycle will automatically be initiated and will take t_{RESTORE} to complete.

$\bar{H}$ AND $\bar{B}$ OPERATION

The STK12C816 provides the $\bar{H}$ and $\bar{B}$ pins for controlling and acknowledging the STORE operations. The $\bar{H}$ pin is used to request a hardware STORE cycle. When the $\bar{H}$ pin is driven low, the STK12C816 will conditionally initiate a STORE operation after t_{DELAY} : an actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\bar{B}$ pin is an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\bar{H}$ is driven low or after an AutoStore™ cycle is requested and $\bar{B}$ is pulled low, are given time to complete before the STORE operation is initiated. After $\bar{H}$ goes low, the STK12C816 will continue SRAM operations for t_{DELAY} . During t_{DELAY} , multiple SRAM READ operations may take place. If a WRITE is in progress when $\bar{B}$ is pulled low it will be allowed a time, t_{DELAY} , to complete. However, any SRAM WRITE cycles requested after $\bar{B}$ transitions low will be inhibited.

The $\bar{H}$ and $\bar{B}$ pins can be used to synchronize multiple STK12C816s while using a single larger capacitor. To operate in this mode the $\bar{H}$ and $\bar{B}$ pins should be connected together and to the $\bar{H}$ and $\bar{B}$ pins from the other STK12C816s. An external pull up resistor to +5V is needed since $\bar{B}$ is an open drain pull down. Do not connect this or any other pull-up to the V_{CAP} pin. The V_{CAP} pins from the other STK12C816 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK12C816s detects a power loss and asserts $\bar{B}$, the common $\bar{H}$ pin will cause all parts to request a STORE cycle (a STORE will take place in those STK12C816s that have been written since the last nonvolatile cycle).

During any STORE operation, regardless of how it was initiated, the STK12C816 will continue to drive the $\bar{B}$ pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the STK12C816 will remain disabled until the $\bar{H}$ pin is brought high.

HARDWARE RESET

A hardware RESET cycle is performed when $\bar{R}$ is brought low, interrupting any cycle in progress with the exception of STORE cycles (assuming t_{HLRL} has been satisfied). $\bar{R}$ interfaces directly to the system reset. RESET, which includes an internally-generated RECALL cycle, takes t_{RLQV} to complete as long as $V_{CAP} > V_{SWITCH}$. If $\bar{R}$ is kept low after the RESET is completed all other pins will remain disabled and the current consumption will be I_{SB2} . Bringing $\bar{R}$ high after the RESET has finished (i.e. $t > t_{RLQV}$) enables the SRAM quickly, within only t_{RHQV} .

Control clock priority is, from highest to lowest: $\bar{R}$; $\bar{Z}$; $\bar{H}$; SRAM control pins. For example, if the $\bar{Z}$ and $\bar{H}$ pins are asserted in unison the part will go to SLEEP rather than STORE.

HARDWARE PROTECT

The STK12C816 offers hardware protection against inadvertent STORE operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$ all externally initiated STORE operations will be inhibited.

AutoStore™ can be completely disabled by tying V_{CCX} to ground and applying +5V to V_{CAP} , as illustrated in Figure 2. This is the data protect mode;

STOREs are only initiated by explicit request using either the software sequence or the $\bar{H}$ pin.

SLEEP MODE

SLEEP mode is initiated by asserting $\bar{Z}$ low. Internally all current loads, including the SRAM array are turned off, reducing current consumption to near zero. This will, of course, cause all SRAM data to be lost. A STORE must be explicitly requested by the user t_{HLZL} before asserting $\bar{Z}$ if the SRAM data is to be preserved. Note that *AutoStore™* and all other operations with the exception of RESET are disabled when $\bar{Z}$ is low. On the rising edge of $\bar{Z}$ a POWER UP RECALL cycle is initiated lasting t_{ZHQV} so long as $V_{CAP} > V_{SWITCH}$.

LOW AVERAGE ACTIVE POWER

The STK12C816 will draw significantly less current when it is cycled at times longer than 30ns. Figure 5, below, shows the relationship between I_{CC} and READ cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, $V_{CC} = 5.5V$, 100% duty cycle on chip enable). Figure 6 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled.

The overall average current drawn by the STK12C816 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READ's to WRITE's; 5) the operating temperature; 6) the V_{CCX} level and; 7) I/O loading.

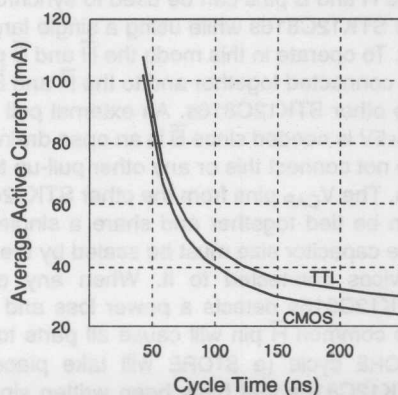


Fig 5: I_{CC} (max) Reads

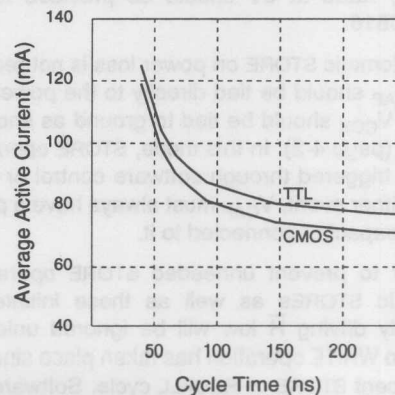


Fig 6: I_{CC} (Max) Writes

ORDERING INFORMATION

STK12C816 - Q 35 I

Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

Q = Plastic Quad Flat Pack

NOTES

ORDERING INFORMATION

STK1535A - Q 35 1

Temperature Range
 0 = Commercial (-40 to 70 degrees C)
 1 = Industrial (-40 to 85 degrees C)

Access Time

35 = 35ns
 35 = 35ns
 45 = 45ns

Package

Q = Plastic Quad Flat Pack

5



STK15C88

32K x 8 AutoStore™ nvSRAM

High Performance CMOS

Nonvolatile Static RAM

PRELIMINARY

FEATURES

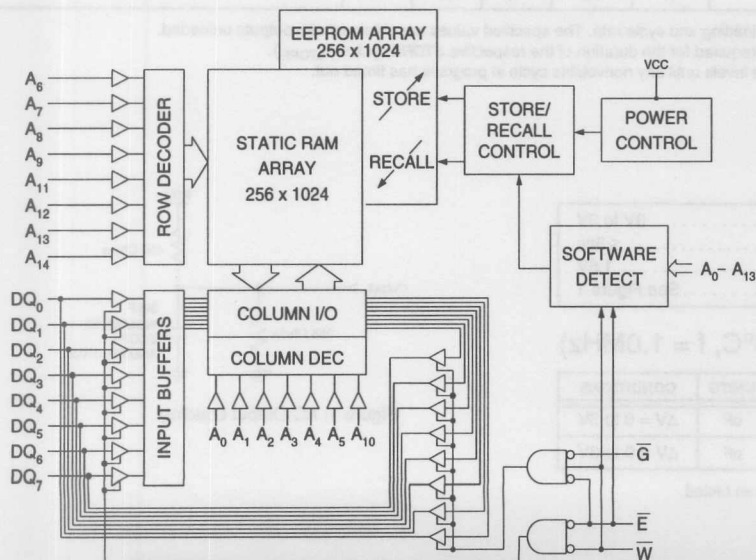
- 25ns, 35ns and 45ns Access Times
- Store to EEPROM Initiated by Software or AutoStore™ on Power Down
- Recall to SRAM Initiated by Software or Power Restore
- 25mA I_{CC} at 200ns Cycle Time
- Unlimited Recalls from EEPROM to SRAM
- 100,000 Store Cycles to EEPROM
- 10 Year Data Retention in EEPROM
- Commercial and Industrial Temp. Ranges
- 28 Pin 600 mil PDIP package

DESCRIPTION

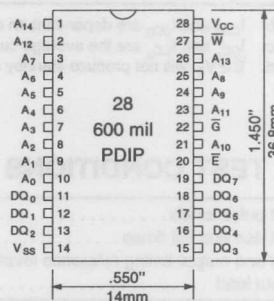
The Simtek STK15C88 is a fast static RAM with a nonvolatile, electrically-erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down using charge stored in system capacitance. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of *STORE* and *RECALL* cycles can also be controlled by entering control sequences on the SRAM inputs.

5

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A ₀ - A ₁₄	Address Inputs
W	Write Enable
DQ ₀ - DQ ₇	Data In/Out
E	Chip Enable
G	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground

STK15C88

ABSOLUTE MAXIMUM RATINGS^a

Voltage on input relative to V_{SS}	−0.6V to ($V_{CC} + 0.5V$)
Voltage on DQ_{0-7}	−0.5V to ($V_{CC} + 0.5V$)
Temperature under bias	−55°C to 125°C
Storage temperature	−65°C to 150°C
Power dissipation	1W
DC output current	15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}^b	Average Current		150 130 110		165 145 125	mA	$t_{AVAV} = 25ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$
I_{CC2}^c	Average Current During STORE		6		7	mA	All inputs Don't Care
I_{CC3}^b	Average VCC Current at $t_{AVAV} = 200ns$		25		25	mA	$\bar{W} \geq (V_{CC} - 0.2V)$ All others cycling, CMOS levels
I_{CC4}^c	Average Current During <i>AutoStore</i> TM Cycle		4		4	mA	All inputs Don't Care
I_{SB1}^d	Average Current (Standby, Cycling TTL Input Levels)		37 33 30		39 35 32	mA	$t_{AVAV} = 25ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 35ns, \bar{E} \geq V_{IH}$ $t_{AVAV} = 45ns, \bar{E} \geq V_{IH}$
I_{SB2}^d	Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to V_{CC} , $\bar{E}$ or $\bar{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	$V_{CC} + .5$	2.2	$V_{CC} + .5$	V	All inputs
V_{IL}	Input Logic "0" Voltage	$V_{SS} - .5$	0.8	$V_{SS} - .5$	0.8	V	All inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
T_A	Operating Temperature	0	70	−40	85	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).

Note d: $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input pulse levels	0V to 3V
Input rise and fall times	≤ 5ns
Input and output timing reference levels	1.5V
Output load	See Figure 1

CAPACITANCE^e ($T_A = 25^\circ C$, $f = 1.0MHz$)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	5	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

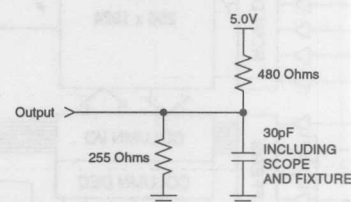


Figure 1: AC Output Loading

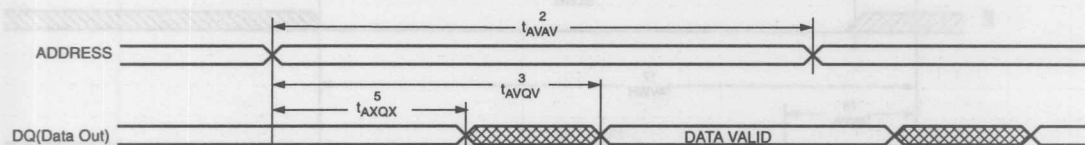
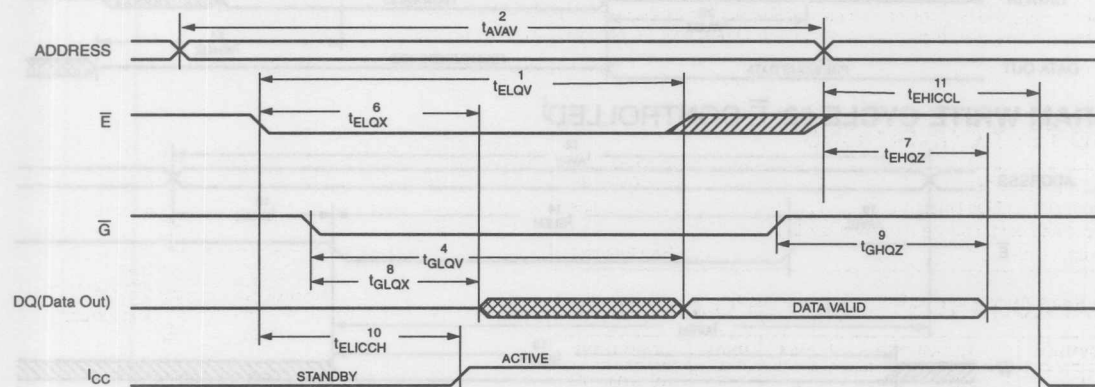
SRAM READ CYCLES #1 & #2
 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS		PARAMETER	STK15C88-25		STK15C88-35		STK15C88-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}^f	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}^g	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}^g	t_{OH}	Output Hold After Address Change	3		3		3		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}^h	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}^h	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}^g	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{d,e}$	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note f: $\overline{W}$ must be high during SRAM read cycles and low during SRAM write cycles.

Note g: I/O state assumes $\overline{E}, \overline{G} \leq V_{IL}$ and $\overline{W} \geq V_{IH}$; device is continuously selected

Note h: Measured $\pm 200mV$ from steady state output voltage

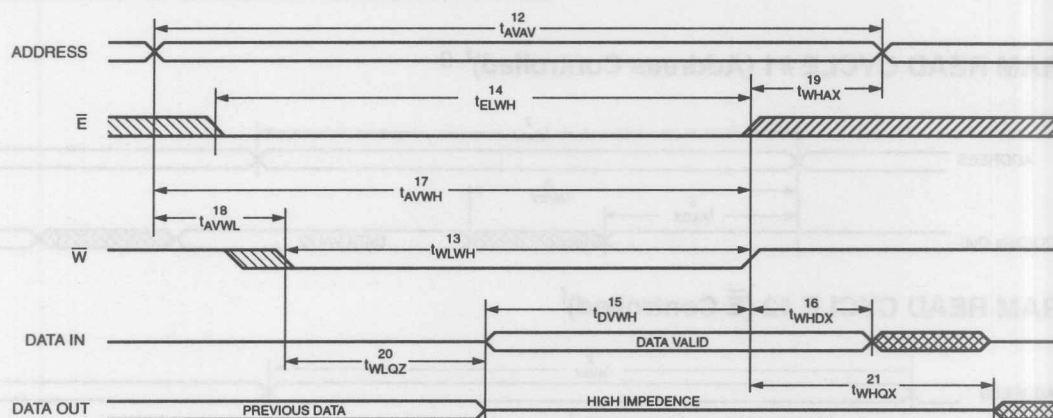
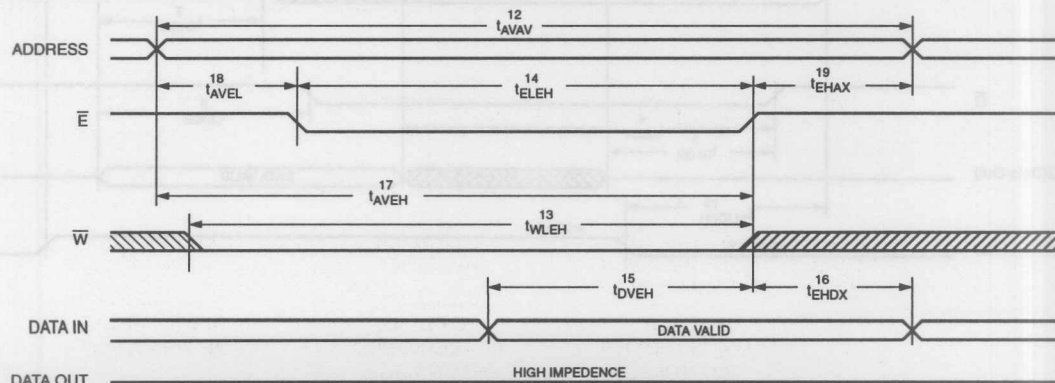
SRAM READ CYCLE #1 (Address Controlled)^{f, g}

SRAM READ CYCLE #2 ($\overline{E}$ Controlled)^f


SRAM WRITE CYCLES #1 & #2
 $(V_{CC} = 5.0V \pm 10\%)$

NO.	SYMBOLS			PARAMETER	STK15C88-25		STK15C88-35		STK15C88-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	$t_{WLOZ}^{h,i}$		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note i: If $\bar{W}$ is low when $\bar{E}$ goes low the outputs remain in the high impedance state.

Note j: $\bar{E}$ or $\bar{W}$ must be $\geq V_{IH}$ during address transitions.

SRAM WRITE CYCLE #1: $\bar{W}$ CONTROLLED

SRAM WRITE CYCLE #2: $\bar{E}$ CONTROLLED


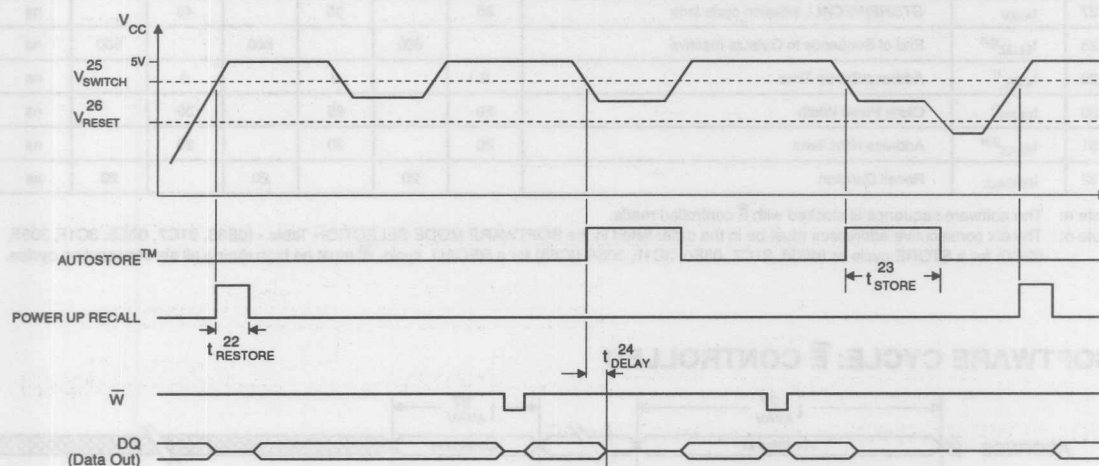
AutoStore™ / POWER-UP RECALL

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK15C88		UNITS	NOTES
	Standard		MIN	MAX		
22	t _{RESTORE}	Power Up RECALL Duration		550	μs	k
23	t _{STORE}	STORE Cycle Duration		10	ms	g
24	t _{DELAY}	Time allowed to Complete SRAM Cycle	1		μs	g
25	V _{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
26	V _{RESET}	Low Voltage Reset Level		3.6	V	

Note k: t_{RESTORE} starts from the time V_{CC} rises above V_{SWITCH}.

AutoStore™ / POWER UP RECALL



POWER-UP
RECALL

BROWN OUT
NO STORE DUE TO
NO SRAM WRITES
NO RECALL
(V_{CC} DID NOT GO
BELOW V_{RESET})

BROWN OUT
AutoStore™
NO RECALL
(V_{CC} DID NOT GO
BELOW V_{RESET})

BROWN OUT
AutoStore™
RECALL WHEN
ABOVE V_{SWITCH}

SOFTWARE MODE SELECTION

$\bar{E}$	$\bar{W}$	A ₁₃ - A ₀ (hex)	MODE	I/O	NOTES
L	H	0E38	Read SRAM	Output data	l,m
		31C7	Read SRAM	Output data	
		03E0	Read SRAM	Output data	
		3C1F	Read SRAM	Output data	
		303F	Read SRAM	Output data	
		0FC0	Nonvolatile <i>STORE</i>	Output high Z	
L	H	0E38	Read SRAM	Output data	l,m
		31C7	Read SRAM	Output data	
		03E0	Read SRAM	Output data	
		3C1F	Read SRAM	Output data	
		303F	Read SRAM	Output data	
		0C63	Nonvolatile <i>RECALL</i>	Output high Z	

Note l: The six consecutive addresses must be in order listed. $\bar{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

Note m: While there are 15 addresses on the STK15C88, only the lower 14 are used to control software modes.

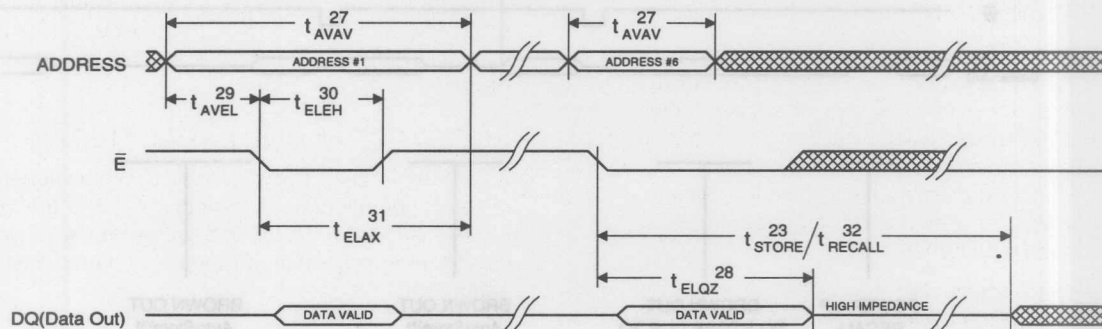
SOFTWARE CYCLES #1 & #2^{n,o}

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK15C88-25		STK15C88-35		STK15C88-45		UNITS
	#1		MIN	MAX	MIN	MAX	MIN	MAX	
27	t _{AVAV}	<i>STORE/RECALL</i> initiation cycle time	25		35		45		ns
28	t _{ELOZ} ^{g,n}	End of Sequence to Outputs Inactive		600		600		600	ns
29	t _{AVEL} ⁿ	Address Set-up Time	0		0		0		ns
30	t _{ELEH} ⁿ	Clock Pulse Width	20		25		30		ns
31	t _{ELAX} ^{g,n}	Address Hold Time	20		20		20		ns
32	t _{RECALL}	Recall Duration		20		20		20	μs

Note n: The software sequence is clocked with $\bar{E}$ controlled reads.

Note o: The six consecutive addresses must be in the order listed in the SOFTWARE MODE SELECTION Table - (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a *STORE* cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a *RECALL* cycle. $\bar{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE: $\bar{E}$ CONTROLLED


DEVICE OPERATION

The STK15C88 is a versatile memory chip that provides several modes of operation. The STK15C88 can operate as a standard 32K x 8 SRAM. It has a 32K x 8 EEPROM shadow to which the SRAM information can be copied, or from which the SRAM can be updated in nonvolatile mode.

NOISE CONSIDERATIONS

Note that the STK15C88 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 μ F connected between DUT V_{CC} and V_{SS} , using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK15C88 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

SOFTWARE NONVOLATILE STORE

The STK15C88 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address	0E38 (hex)	Valid READ
2. Read address	31C7 (hex)	Valid READ
3. Read address	03E0 (hex)	Valid READ
4. Read address	3C1F (hex)	Valid READ
5. Read address	303F (hex)	Valid READ
6. Read address	0FC0 (hex)	Initiate STORE cycle

The software sequence is clocked with $\overline{E}$ controlled reads.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed:

1. Read address	0E38 (hex)	Valid READ
2. Read address	31C7 (hex)	Valid READ
3. Read address	03E0 (hex)	Valid READ
4. Read address	3C1F (hex)	Valid READ
5. Read address	303F (hex)	Valid READ
6. Read address	0C63 (hex)	Initiate RECALL cycle

STK15C88

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AutoStore™ OPERATION

The STK15C88 uses the intrinsic system capacitance to perform an automatic store on power down. As long as the system power supply takes at least t_{STORE} to decay from V_{SWITCH} down to 3.6V the STK15C88 will safely and automatically store the SRAM data in EEPROM on power-down.

In order to prevent unneeded STORE operations, automatic STORE will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place.

POWER UP RECALL

During power up, or after any low power condition ($V_{\text{CC}} < V_{\text{RESET}}$) an internal recall request will be latched. When V_{CC} once again exceeds the sense

voltage of V_{SWITCH} , a RECALL cycle will automatically be initiated and will take t_{RESTORE} to complete.

HARDWARE PROTECT

The STK15C88 offers hardware protection against inadvertent STORE operation during low voltage conditions. When $V_{\text{CC}} < V_{\text{SWITCH}}$ all Software STORE operations will be inhibited.

LOW AVERAGE ACTIVE POWER

The STK15C88 draws significantly less current when it is cycled at times longer than 30ns. Figure 2, below, shows the relationship between I_{CC} and READ cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, $V_{\text{CC}} = 5.5\text{V}$, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK15C88 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READ's to WRITE's; 5) the operating temperature; 6) the V_{CC} level and; 7) I/O loading.

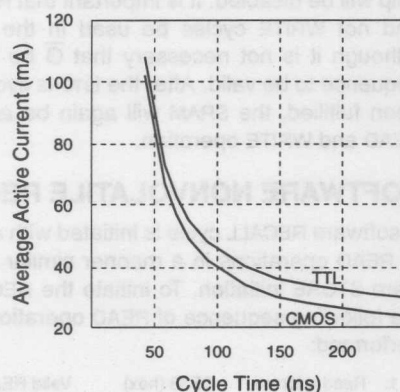


Fig 2: Icc (max) Reads

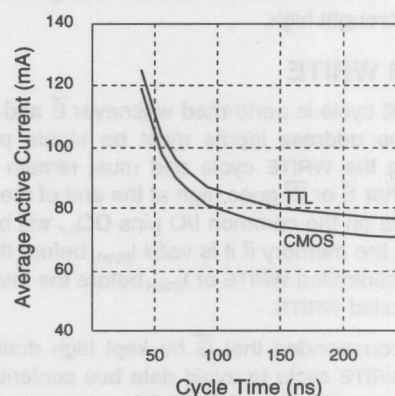


Fig 3: Icc (Max) Writes

ORDERING INFORMATION

STK15C88 - W 25 I



Temperature Range

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

W = Plastic 28 pin 600 mil PDIP

Application Notes 6



SIMTEK

Common nvSRAM Questions

Simtek Corporation manufactures a complete family of high speed, high performance nonvolatile Static Random Access Memories (nvSRAM). Simtek's entire product line is guaranteed nonvolatile for a minimum of 10 years, without any source of external power, special handling, storage or care. Simtek nvSRAMs contain no internal batteries, capacitors, or power sources. Data is *Stored* into integral EEPROM (Shadow ROM) in parallel from the high speed SRAM, resulting in short nonvolatile *Store* times. *Store* or *Recall* operations are initiated upon execution of user command, or upon loss of power with the *AutoStore™* versions.

1. What is the difference between a standard fast SRAM and the nvSRAM?

Simtek nvSRAMs combine the ease of use of a standard fast SRAM with the nonvolatility of EEPROM. Within each SRAM cell is an EEPROM cell that can be *Recalled* from or *Stored* to the SRAM. A block diagram of the Simtek nvSRAM architecture is shown in Figure 1.

Simtek nvSRAMs are available in commercial (0° to 70° C), industrial (-40° to 85° C), and military (-55° to 125° C) temperature ranges. Performance specifications vary slightly with the various temperature ranges listed, and specific data sheets should be consulted for exact specifications. All performance data referred to in this application note is for commercial rated components only.

Nonvolatile STORE Operation

During a *Store* operation, data is transferred from SRAM to EEPROM in parallel (e.g., for an 8K x 8 STK11C68, the data in all 64K SRAM cells is *Stored* in parallel to the 64K EEPROM cells). This allows data to be *Stored* safely in a maximum of 10ms. Nonvolatile *Stores* can be initiated in three ways: *Hardware Store*, *Software Store*, or *AutoStore™*, depending on the family of component selected.

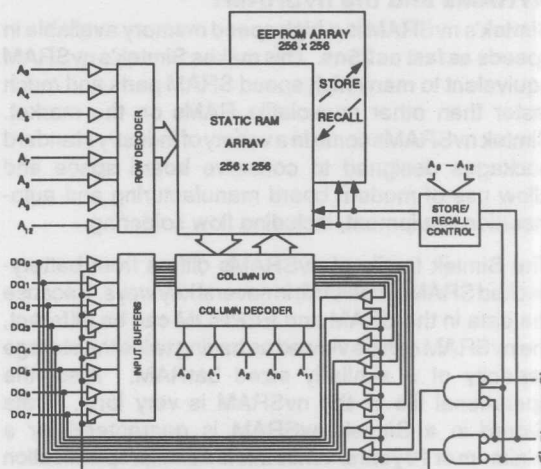


Figure 1
Example Block Diagram (STK11C68)

Recall Operations

A *Recall* operation transfers data from EEPROM to SRAM, in parallel, in a maximum of 20 μ s. *Recalls* can be initiated in 3 ways: *Software Recall* or *Hardware Recall* depending on the family of component selected, and all Simtek nvSRAMs automatically *Recall* stored data to SRAM upon power-up.

SRAM Operations

The hardware interface to the nvSRAM is nearly identical to common high speed SRAMs. The three nvSRAM control signals, $\overline{G}$ (output enable), $\overline{E}$ (chip enable), and $\overline{W}$ (write enable), are used in the same manner as the functionally equivalent pins on common fast SRAM. Depending on the Simtek part selected, the design engineer may have to accommodate the hardware *Store/Recall* start pin $\overline{NE}$ (Nonvolatile Enable), and the loss of one Chip Select pin that is

found on most common SRAMs. Since the hardware or software sequences necessary to initiate nonvolatile operations use the standard SRAM control pins, very few hardware modifications are required to use nvSRAMs in place of standard SRAMs. When $\bar{E}$ is deasserted (held high) the chip goes into the standby (low power) power consumption mode.

2. What is the difference between other NVRAMs and the nvSRAM?

Simtek's nvSRAM is a high speed memory available in speeds as fast as 25ns. This makes Simtek's nvSRAM equivalent to many high speed SRAM parts and much faster than other nonvolatile RAMs on the market. Simtek nvSRAMs come in a variety of industry standard packages designed to conserve board space and allow use of modern board manufacturing and auto-insertion equipment, including flow soldering.

The Simtek family of nvSRAMs differs from battery-backed SRAMs (batRAM) in several key ways. Because the data in the SRAM and EEPROM can be different, the nvSRAM can be viewed as having twice the storage capacity of a similarly sized batRAM. Also, the operational life of the nvSRAM is very long. Data Stored in a Simtek nvSRAM is guaranteed for a minimum of 10 years. While this is a similar specification to most batRAM products on the market, at the end of 10 years the batRAM is no longer usable and must be discarded. Simtek's parts on the other hand can be re-*Stored* and are good for another 10 years after each *Store*. In addition, because the nvSRAM contains just a single die it will function over a wider environmental range than hybrid battery/die parts. In light of the "green laws" that are sweeping the world the problem of disposing of an environmental toxin (lithium) is avoided all together.

3. What is the difference between EEPROM and the nvSRAM?

Reading and Writing an EEPROM and the nvSRAM require controlling the same three signals ($\bar{E}$, $\bar{W}$, $\bar{G}$) in a similar fashion. The difference however is that Write operations on the nvSRAM (which are to the SRAM section) take only 25ns, while typical EEPROMs require 10ms to perform a Write. Of course a single 10ms *Store* operation is required at some time if the data written into the SRAM is to be made nonvolatile.

The Simtek nvSRAM family offers access times much faster than any EEPROM on the market. Since all of the EEPROM cells within the nvSRAM are *Stored* in

parallel, the full chip programming time is much shorter than for standard EEPROM. For example the STK10C68 8K x 8 nvSRAM can be completely written and programmed (a *Store* cycle) in 10ms, while a typical 28C64 8K x 8 EEPROM requires almost 2.5 seconds for the same operation.

The Simtek nvSRAM performs an automatic *Recall* upon power-up, so it may be used as a read-mostly memory, the function that conventional EEPROM and Flash memories perform. In order to support these read-only or read-mostly applications, a number of PROM programmer manufacturers support the nvSRAM on their programmers.

4. Why are there different versions of nvSRAM?

There are three distinctly different nvSRAM architectures available: the *Hardware Store*, the *Software Store*, and the *AutoStore™*. Each family is uniquely designed to fill a specific high technology niche. This helps the digital design engineer reduce size and cost, and to overcome technical obstacles that plague the design of many nonvolatile memory systems.

STK10C "Hardware Store" nvSRAM

The Simtek 10C "Hardware Store" family is designed to easily replace SRAM devices in existing designs with minimal hardware changes. The STK10C family uses the JEDEC standard pinout that adds an $\bar{N\bar{E}}$ (nonvolatile enable) pin to the standard SRAM pinout. If the $\bar{N\bar{E}}$ line is asserted during either a Read or Write, a *Recall* or *Store* operation will be initiated respectively. Note that all four control pins must be in the correct state to initiate nonvolatile cycles.

STK11C "Software Store" nvSRAM

The STK11C "Software Store" family is designed to replace SRAM devices in existing designs with no hardware changes required. *Store* and *Recall* operations are initiated by Reading a precise sequence of six addresses in order, with no intervening access to other locations. This allows the design engineer to add nonvolatility to an existing design without requiring hardware changes. Only a software change is required to initiate nonvolatile cycles. By Reading the 6 addresses in sequence (instead of Writing to the address locations), the design engineer avoids the danger of corrupting the data stored at the nonvolatile control SRAM addresses. The probability of accidentally initiating a nonvolatile cycle by randomly accessing the nvSRAM is less than 1 in 10^{23} .

STK12C "AutoStore™" nvSRAM

The STK12C family is designed to provide the ease of use and data security of battery-backed SRAM without the environmental issues, speed limitations and non-standard package sizes of batRAM. At the same time, the nvSRAM is more reliable. Call Simtek for data and test conditions.

Data is automatically *Stored* when system V_{CC} drops below approximately 4.2 volts, and is guaranteed nonvolatile for a minimum of 10 years. The 12C family is designed to be a functional replacement for batRAM, low density FLASH, and system battery backed-up memory. The 12C family's high speed (25ns Read and Write) makes it an ideal replacement for EEPROM/SRAM combination systems that require more board space and consume higher power. The 12C family also incorporates Hardware (10C/20C) and Software (11C) *Store* capability, making the STK12C the most versatile and reliable nonvolatile memory solution available today.

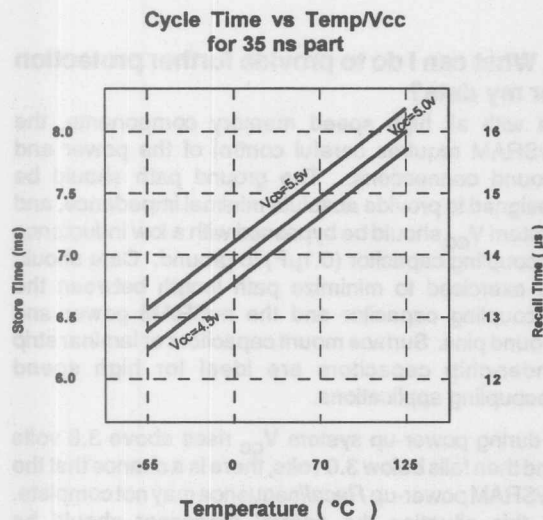


Figure 2
Typical Store/Recall Times

5. How do the *Store* and *Recall* times vary over the operating conditions?

All parts are tested over the specified temperature and voltage ranges to insure that the data sheet parameters

are met. Typical *Store* and *Recall* times will vary with both temperature and voltage as well as from part to part. Typical times are shown in *Figure 2*.

6. Can I Read or Write the SRAM during a *Store* or *Recall* operation?

During a *Store* or *Recall* operation, the nvSRAM is unavailable to the system. All levels and transitions on the input control pins are ignored and all data pins are tri-stated. After the nonvolatile cycle is completed, a Read or Write cycle can be initiated immediately by the proper assertion of the control lines.

Depending on the family of nvSRAM used, two different methods may be employed to monitor completion of a nonvolatile cycle. On some *AutoStore™* parts, a bi-directional I/O pin, HSB (Hardware Store/Busy), is used to indicate when a nonvolatile *Store* cycle is in progress. This pin is internally driven low whenever a *Store* is in progress. The HSB line may also be used as an input control line to initiate a *Store* operation. This is accomplished by externally driving the line low for a minimum of 250ns. After that time internal circuitry will hold the HSB line low for the duration of the *Store* cycle. A pull-up resistor should be used on the HSB line to minimize the chance of noise-initiated *Store* operations. The value of the pull-up should be carefully selected so as not to overpower the internal output driver in the 12C. If the HSB line cannot be internally driven low, the 12C will not perform nonvolatile *Store* operations. On the STK12C88 (32K x 8) and STK12C816 (16K x 16) the B open drain output goes active (low) during *Store* cycle.

If the 11C or 10C families are being used, and it is necessary to monitor completion of the nvSRAM nonvolatile cycle, a pull-up resistor may be connected to one of the data pins, as shown in *Figure 3*. After a *Store* or *Recall* is started, the processor can repeatedly read a location in the nvSRAM that contains a logic zero. While the nvSRAM is busy, the resistor will pull the data line high. When the nonvolatile cycle is completed, a Read operation that is performed on that address will drive the line low signaling the processor that the cycle has completed.

7. What protection does the nvSRAM provide against Inadvertent *Stores*?

Simtek has built-in a number of safeguards to insure that inadvertent *Store* operations are avoided. Each family takes a different approach to ensuring data

safety and will be described below.

The STK10C Family

On the STK10C, a transition is necessary on one of the control lines before a *Store* operation can be initiated. Therefore, system control circuitry can hold the $\overline{NE}$, $\overline{G}$, $\overline{W}$, and $\overline{E}$ lines in the *Store* or *Recall* state for greater than 10ms without fear that the part will initiate a second nonvolatile operation. If the necessary transition has occurred, a nonvolatile operation will successfully start if the control lines are held in the proper state for greater than or equal to one SRAM cycle time. If the pins are held in the *Store* command state for longer than 10ms, the $\overline{E}$ line should be de-asserted first in order to prevent an unintentional SRAM write cycle from occurring.

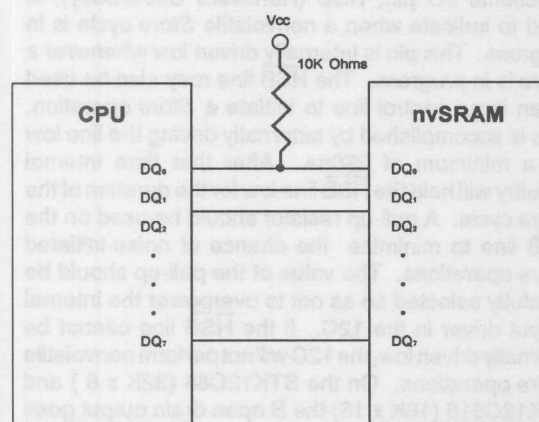


Figure 3
Early Termination Detection Circuit

The STK11C Family

The STK11C family of parts provides very high data security and protection from unwanted *Store* operations by requiring the sequential reading of six specific addresses to start nonvolatile operations. The odds of accidentally starting a nonvolatile operation on an STK11C68 by randomly accessing the part is 1 in 3×10^{23} .

The STK12C Family

The STK12C family incorporates a number of safety features in its design. Software *Store* protection is similar to the 11C family and has the same high degree of data safety. Hardware Initiated or *AutoStore*™

operations require that at least one *Write* operation take place since the last *Store*. This feature ensures that noise on the $\overline{HSB}$ line or a fluctuating power bus will not initiate a second *Store* operation that could corrupt or destroy the integrity of the *Stored* data. Low voltage *Store* protection is provided on-board the chip to ensure that all *Store* operations are inhibited whenever V_{cap} is lower than V_{switch} . This guarantees that a *Store* operation cannot be started that won't have time to finish before chip power falls below approximately 3.6 volts.

During power-up, the system can execute Reads and Writes until proper reset sequences are executed. All Simtek nvSRAM products automatically initiate a 20μs *Recall* cycle once power is adequate.

It is advised that embedded microprocessors and control circuitry be held in reset until system V_{CC} reaches approximately 4.5 volts and their output lines are quiet. Due to the high speed of the Simtek nvSRAM, random uncontrolled noise on the address, data, and control lines may result in corruption of the *Recalled* data unless care is taken during the system design process.

8. What can I do to provide further protection for my data?

As with all high speed memory components, the nvSRAM requires careful control of the power and ground connections. The ground path should be designed to provide absolute minimal impedance, and system V_{CC} should be bypassed with a low inductance decoupling capacitor (0.1μF) to ground. Care should be exercised to minimize path length between the decoupling capacitor and the nvSRAM power and ground pins. Surface mount capacitors or laminar strip under-chip capacitors are ideal for high speed decoupling applications.

If during power-up system V_{CC} rises above 3.8 volts and then falls below 3.0 volts, there is a chance that the nvSRAM power-up *Recall* sequence may not complete. In this situation the control processor should be programmed to perform an explicit *Recall* during its power-on reset sequence. If the system is designed with a sufficiently long power on Reset, such that the processor does not start to execute until V_{CC} has stabilized, this problem can be to a large part eliminated.

In applications where the nvSRAM input lines may see noisy or floating inputs, it may be necessary to use pull-up and pull-down resistors to avoid unwanted SRAM

Read or Write operations. $\overline{NE}$, $\overline{W}$, and $\overline{E}$ should be pulled high, while $\overline{G}$ should be pulled low. This configuration will provide maximum protection against unwanted *Store* operations.

9. What is the difference between retention and endurance?

Retention is a measure of how long data will be safely saved in the nonvolatile cells. Remember that retention is measured from the time of the *Store*. Data *Stored* 15 years from now will still be valid 25 years from now.

Endurance is a measure of the number of times that data can be *Stored* into nonvolatile memory (EEPROM) before the cell wears out. In the nvSRAM, the user performs Writes to the SRAM portion of the chip, which has no wear-out mechanism, and can effectively be accessed an unlimited number of times. The nonvolatile *Store* operation utilizes the EEPROM cells and is guaranteed a minimum of 100,000 times. If a *Store* operation is performed once each time the system is powered down, and the system is powered down 5 times per day, more than 50 years will elapse before the nvSRAM's endurance specification is exceeded. Data may be *Recalled* from nonvolatile memory an unlimited number of times with no danger of the part wearing out.



Address Sequence Generation on the STK11C and STK12C

Simtek's nvSRAMs combine fast SRAM and EEPROM on a single chip in a shadow memory configuration. The parallel transfer of data from EEPROM to SRAM, a *RECALL* cycle, takes place under explicit user control. The *STORE* operation, which performs a parallel transfer of data from the SRAM to EEPROM, also occurs when specified by the user.

On the STK11C versions of the nvSRAM, *STORE* and *RECALL* operations are initiated by performing a sequence of SRAM *read* cycles from six specific locations. An access to a different address during this sequence, or repeated accesses to the same address will prevent the *STORE* or *RECALL* from being initiated.

In order to achieve fast asynchronous SRAM read performance, the nvSRAM detects changes on the address pins with $\bar{E}$ low and $\bar{W}$ high and initiates the internal *read* circuitry after that address state is stable for 5ns. This high speed operation requires that the address and control sequencing be carefully controlled if the 6 address sequence is to properly initiate a nonvolatile cycle.

Only $\bar{E}$ controlled read accesses may be used for the 6 addresses in the STK11C sequences, as shown in *Figure 1*. $\bar{E}$ must be held high while the addresses are changing. After the addresses have settled, $\bar{E}$ should be held low for the entire access time, during which no address should change state. Whenever $\bar{E}$ is high, the nvSRAM is disabled and any address transitions will be ignored.

The state of the $\bar{G}$ pin is ignored during the 6 address sequence. The $\bar{G}$ pin is only used to disable the outputs and cannot be used in the place of $\bar{E}$ to strobe the valid addresses. It is recommended that the $\bar{G}$ pin

be held high during the address sequence to keep the outputs in the high-Z state and reduce noise generated by the output drivers.

Excessive noise on the control pins that might be interpreted as spurious accesses to the nvSRAM must be prevented. If for instance, $\bar{E}$ goes low (below V_{IL}), but exhibits sufficient bounce that it then rises above V_{IL} before falling below it again, the part may "see" two accesses. Since both of these accesses will be to the same address, the address sequence necessary to cause a *STORE* or *RECALL* cannot occur. Note that this noise can be caused either by noise on the control signal itself, or by noise (bounce) on the power or ground pins. The shaded regions of *Figure 2* show areas of questionable validity.

Proper noise control, important with all high speed integrated circuits, must be exercised throughout the board design. Noise, whether coupled from drive IC power supplies, adjacent wires or traces, ringing or other sources must be kept to a minimum with appropriate techniques. Proper capacitive bypassing of the power supply pins should be observed, using bypass capacitors having minimal internal resistance and inductance located as close as possible to the actual chip.

Simtek's *AutoStore*TM (STK12C) nvSRAMs can also be operated in "Software *STORE*" mode. This versatile family of high performance nonvolatile memory offers the flexibility of automatic power-down *STORE* (*AutoStore*TM), the ease of use of "Hardware *STORE*", and the data security of Software *STORE*. The "Software *STORE*" operation for the STK12C is identical to the STK11C.

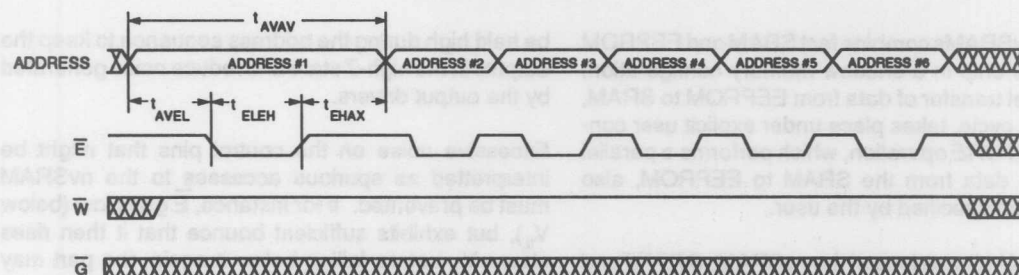


Figure 1:
STK11C Sequence Timing

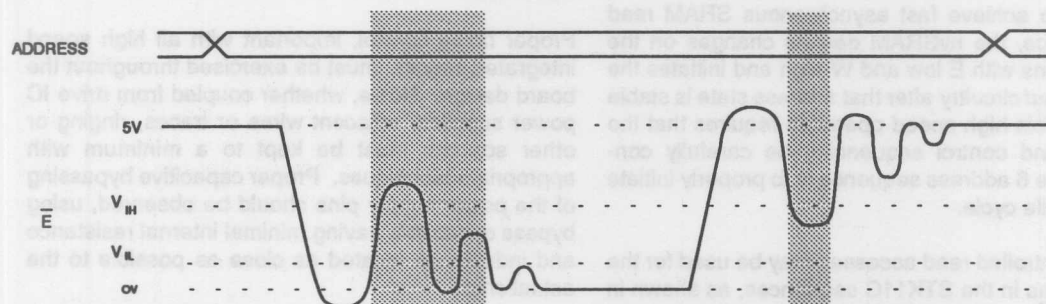


Figure 2:
Clock Noise Causing Spurious Accesses



Comparison of SIMTEK nvSRAM vs. Battery Back-up SRAMs

This document summarizes two options for nonvolatile memory: Simtek Corporation's nvSRAM and battery backed-up SRAM from other manufacturers.

What is a battery backed-up SRAM?

Embedded in the package of a battery backed-up SRAM is a lithium energy source and circuitry that switches power to the battery when a voltage drop is detected.

When the supply voltage dips below some specified level, the internal energy source is switched on to sustain the memory until V_{CC} returns to a valid condition.

A functional diagram is shown below.

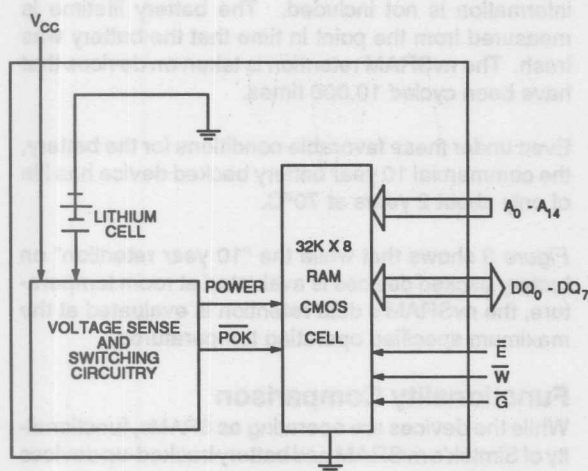


Fig. 1 Battery Backed-up SRAM Functional Diagram*

* Diagram generated from SGS-Thomson Microelectronics Datasheet MK48Z30, 30A

What is an nvSRAM?

Simtek's nvSRAM is a high performance SRAM with a shadow EEPROM.

Information is made nonvolatile by loading it into the EEPROM which takes less than 10ms. This STORE operation is initiated by signaling an input pin (STK10C family), by executing a software sequence (STK11C family), or automatically upon power loss (AutoStore™ family). The information is loaded back into the SRAM automatically on power-up or by using the hardware or software function.

A functional diagram of the device is shown below.

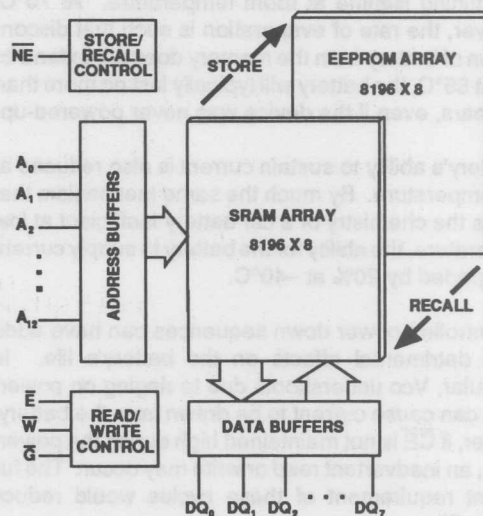


Fig. 2: nvSRAM Functional Diagram

Data Retention vs. Product Lifetime

Data retention time is referenced to when the data is stored, while product lifetime refers to when the device was manufactured. The nvSRAM has a fixed *data retention*, while the battery backed-up device has a fixed *product lifetime*.

Ten year data retention is guaranteed on the nvSRAM after each of the 100,000 *STORE* operations. Consider, for instance, a scenario where an nvSRAM *STORE* is performed before a system is powered down, after which the system power is shut off once per day. The nvSRAM's 100,000th *STORE* cycle will be performed after about 274 years. The data transferred to the EEPROM at that point will then be retained for 10 years from that time. The product life of the nvSRAM in this scenario is 284 years.

The battery backed-up SRAM ceases to function as nonvolatile memory after the battery loses its charge, typically 5-10 years in commercial systems.

Battery lifetime is reduced by two major factors: current drain from memory circuits, and evaporation of electrolyte. The first of these depends on the current requirements of the memory, and is the predominant factor determining lifetime at room temperature. At 70°C, however, the rate of evaporation is such that disconnection of battery from the memory does not extend its life. At 85°C, the battery will typically last no more than two years, even if the device was never powered-up.

A battery's ability to sustain current is also reduced at low temperature. By much the same mechanism that makes the chemistry of a car battery inefficient at low temperature, the ability for the battery to supply current is degraded by 20% at -40°C.

Uncontrolled power down sequences can have additional detrimental effects on the battery's life. In particular, *Vcc* undershoots due to ringing on power-down can cause current to be drawn from the battery. Further, if *CE* is not maintained high during the power-down, an inadvertent read or write may occur. The full current requirement of these cycles would reduce battery life.

The nonvolatile memory element in an nvSRAM is an EEPROM cell. This cell consists of a nitride insulator and a thin oxide insulator sandwiched between a conductor and the silicon surface. The programming charge is stored in the nitride insulator. Injection of a charge into the nitride is controlled by the electric field

between the conductors.

Data retention is determined by the insulator's ability to hold this charge. As the cell is cycled or the temperature increased, the insulator will tend to permit more charge to leak. The data retention of an nvSRAM is determined by the number of *STORE* operations which have been performed, and the average temperature at which the device was stored.

All Simtek nvSRAM devices are tested with a temperature acceleration factor that will guarantee the full retention specification on the last specified *STORE* cycle when maintained at maximum operating temperature.

Because the mechanisms effecting data retention are so different between the nvSRAM and a battery backed device, they are difficult to compare. One effective way is to look at a plot of mean time to failure. *Figure 3* indicates how long it takes before 1% of the total population of devices fail at any given temperature.

The plots for the battery backed-up devices include only the evaporation of electrolyte as the degrade mechanism. Actual data retention will be worse, since current drawn from the battery to maintain the memory information is not included. The battery lifetime is measured from the point in time that the battery was fresh. The nvSRAM retention is taken on devices that have been cycled 10,000 times.

Even under these favorable conditions for the battery, the commercial 10 year battery backed device has life of only about 2 years at 70°C.

Figure 3 shows that while the "10 year retention" on battery backed devices is evaluated at room temperature, the nvSRAM's data retention is evaluated at the maximum specified operating temperatures.

Functionality Comparison

While the devices are operating as SRAMs, functionality of Simtek's nvSRAM and battery backed-up devices are identical.

Simtek's nonvolatile SRAM is available in 25ns through 55ns speed bins. Battery backed-up devices must optimize the standby power consumption to maximize retention, and must sacrifice access time in the process. The fastest 64K battery backed-up SRAM devices are 70ns to 100ns.

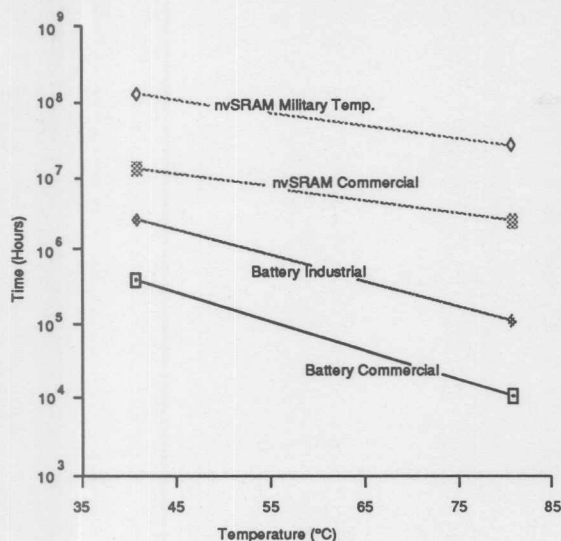


Figure 3: Mean Time to Failure

1. Output Current

Battery: Most battery backed-up specifications are 1mA and 2mA. Lower output drive current will translate to slower access times with high output loads.

nvSRAM: Output current capabilities on the nvSRAM are higher than on some battery backed devices. The nvSRAM outputs pin drive 4mA and 8mA for a logic 1 and logic 0, respectively.

2. Device Functionality on Power-down

Battery: Chip Enable must be maintained at a high logic level in order to avoid inadvertent reads or writes during power-down. During power-down conditions the battery output voltage could drop below levels needed to sustain the data in the memory and could draw currents reducing battery life. The Dallas Semiconductor data book recommends the use of a power monitor chip for this purpose.

nvSRAM: The *AutoStore*™ nvSRAM will detect a voltage loss and automatically STORE the SRAM contents into the EEPROM. The "Hardware STORE" family of nvSRAMs can be used with external circuitry to provide a signal for the STORE operation. The appropriate address sequence can be used with Simtek's Software STORE family of nvSRAM to initialize the STORE sequence.

3. Conditions on V_{CC} During Power-down

Battery: V_{CC} must drop from 4.74V (or from 4.25V

depending on the device) to 0V in no less than 300μs. The system requires a power supply slew rate which meets this specification.

nvSRAM: The *AutoStore*™ nvSRAM recognizes a voltage loss at approximately 4.3V and automatically transfers the SRAM contents into EEPROM. The Hardware and Software STORE families of nvSRAM require that a voltage of 4.5V or higher be maintained for at least 10ms after the STORE cycle has been initiated.

4. Negative Voltages on Pins

Battery: The system design must guarantee that voltages do not ring to less than -0.3V on any pins. Doing so would forward bias the ESD devices, thereby drawing a current too large for the battery to sustain, reducing battery lifetime. The Dallas Semiconductor data book recommends that the SRAM pins be shunted with diodes for this purpose.

nvSRAM: There are no special conditions that must be met for negative voltage ringing. Even if the ESD devices do forward bias, data integrity is maintained.

5. Device Functionality on Power-up

Functionally, the power-up requirements on the nvSRAM and the battery backed device are identical. The nvSRAM automatically transfers data from the EEPROM to the SRAM upon power-up, after which the device is ready for SRAM operation. A battery backed-up SRAM will automatically switch from the lithium source to the V_{CC} supply, after which the device is ready for SRAM operation. In both cases, monotonic rise of V_{CC} is needed. The difference between them is as follows:

Battery: Chip Enable must be maintained high for at least 125ms after power-up. While $\overline{CE}$ is high, the chip cannot be read or written. There are some devices where this time is reduced to 2ms. Even this length of delay would likely require special attention in the system's bootstrap sequence.

nvSRAM: There is no special requirement on $\overline{E}$ during power-up. Data is available 25μs after power-up.

6. Board Space

Battery: Systems implementing batteries must sacrifice board space in height or width (or both) to accommodate for the battery. Typical packaging ranges from 0.360" x 600mil to 0.451" x 720mil.

nvSRAM: Simtek's nvSRAM DIP packaging is available in 0.160" x 300mil, allowing the nvSRAM to be substituted for SRAM without increasing board space.

depending on the device) to 0V in no less than 300µs. The system regulates a power supply slow rate which meets this specification.

nvSRAM: The *AutoStore™* nvSRAM recognizes a voltage loss at approximately 4.2V and automatically transfers the SRAM contents into EEPROM. The Hard-ware and Software STORE families of nvSRAM require that a voltage of 4.5V or higher be maintained for at least 10ms after the STORE cycle has been initiated.

4. Negative Voltages on Pins: The system design must guarantee that voltages do not rise to less than -0.3V on any pins. Doing so would forward bias the ESD devices, thereby drawing a current too large for the battery to sustain, reducing battery lifetime. The Dallas Semiconductor data book recommends that the SRAM pins be grounded with diodes for this purpose.

nvSRAM: There are no special conditions that must be met for negative voltage timing. Even if the ESD device is forward biased, data integrity is maintained.

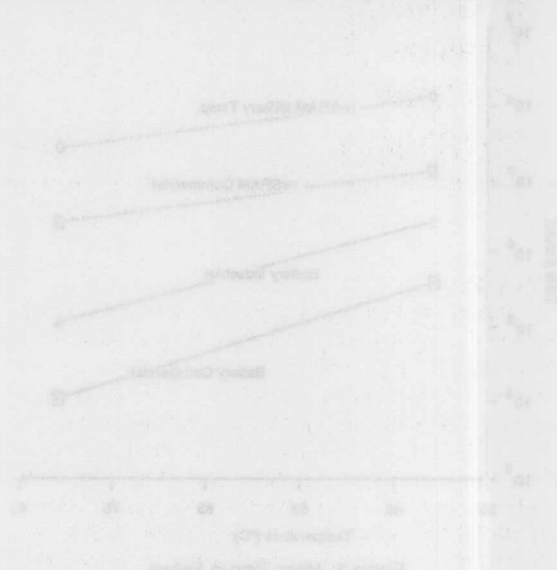
5. Device Functionality on Power-up: Functionally, the power-up requirements on the nvSRAM and the battery backed device are identical. The nvSRAM automatically transfers data from the EEPROM to the SRAM upon power-up, after which the device is ready for SRAM operation. A battery backed nvSRAM will automatically switch from the SRAM output to the Vcc supply after which the device is ready for SRAM operation. In both cases, minimum time of Vcc is needed. The difference between them is as follows:

Battery: Chip Enable must be maintained high for at least 125ms after power-up. While CE is high, the chip cannot be read or written. There are some devices where this time is reduced to 5ms. Even this length of delay would likely require special attention in the system's bootstrap sequence.

nvSRAM: There is no special requirement on CE during power-up. Data is available 25µs after power-up.

6. Board Space: Systems implementing batteries must account board space in height (or width for battery) as well as area for the battery. Typical packaging ranges from 0.350" x 0.600" to 0.451" x 0.750".

nvSRAM: Simtek's nvSRAM chip packaging is available in 0.180" x 0.060", allowing the nvSRAM to be substituted for SRAM without increasing board space.



1. Output Current: Most battery backed-up specifications are 1mA maximum. Lower output current will translate in shorter access times with high output loads.

nvSRAM: Output current capabilities on the nvSRAM are higher than on some battery backed devices. The nvSRAM outputs pin drive 4mA and 8mA for a logic 1 and logic 0, respectively.

2. Dallas Functionality on Power-down: Battery: Chip Enable must be maintained at a high logic level in order to avoid inadvertent reads or writes during power-down. During power-down conditions the battery output voltage could drop below levels needed to sustain the data in the memory and could draw current reducing battery life. The Dallas Semiconductor data book recommends the use of a power monitor chip for this purpose.

nvSRAM: The *AutoStore™* nvSRAM will detect a voltage loss and automatically STORE the SRAM contents into the EEPROM. The Hardware STORE family of nvSRAMs can be used with external circuitry to provide a signal for the STORE operation. The appropriate address sequence can be used with Simtek's Battery STORE family of nvSRAM to initiate the STORE sequence.

3. Conditions on Vcc during Power-down: Battery: Vcc must drop from 4.74V for non-4.2V



Incoming Test Procedures for the STK12C68

Synopsis

It is possible to observe a false failure of STK12C68 devices during incoming test if the Chip Enable ($\overline{CE}$) pin is brought high before power is applied to the devices. While this does not harm the device or disturb the nonvolatile data in any way, it will appear that the SRAM will not read/write correctly for the length of a *RECALL* cycle (approximately 15 microseconds at 5V at room temperature). The failure will only occur on the first SRAM test after the device arrives at the test location; after this first test, the part will function normally as long as it remains socketed.

Discussion

A node in an internal test mode control circuit connected to the address pin A9 can be pulled high by static charge when the part is handled just prior to insertion for test. If this internal mode is high *when the part is powered up with $\overline{CE}$ high*, the first time $\overline{CE}$ is brought low, the part will perform a *RECALL* - disabling the SRAM, making it appear as though the part has failed the SRAM read or write. Bringing $\overline{CE}$ low discharges the internal node allowing the device to function normally.

Since this node is pulled low whenever $\overline{CE}$ is low, if the part is powered up with $\overline{CE}$ low, the part will operate normally. Once the part is powered up, this node will leak low even when $\overline{CE}$ is high. Further, in a system application, since the part is either socketed or soldered in place, this node cannot be brought high.

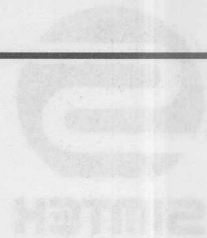
In a testing environment, we have observed this failure mode during manual insertion testing as well as during testing in handlers. Plastic packaged devices sliding through a handler can pick up enough static to cause the problem.

Suggestions for Incoming Test

The problem can be avoided by bringing up $\overline{CE}$ after Vcc rises or by waiting 20 microseconds (the *RECALL* time specification) after the first time $\overline{CE}$ is brought low and then testing the SRAM again.

Note that bringing Vcc up with $\overline{CE}$ low and $\overline{WE}$ low (assuming HSB is high) will cause an SRAM write as soon as the part has completed its power-up *RECALL*; overwriting the SRAM after the power-up *RECALL* can be avoided by bringing $\overline{CE}$ high before Vcc is brought up.

Incoming Test Procedures for the STK1208



Since this node is pulled low whenever $\overline{CE}$ is low, if the part is powered up with $\overline{CE}$ low, the part will operate normally. Once the part is powered up, this node will sink low even when $\overline{CE}$ is high. Further, in a system application, since the part is either powered or not, based in place, this node cannot be brought high.

In a testing environment, we have observed this failure mode during manual function testing as well as during testing in handlers. Plastic packaged devices sitting through a handler can pick up enough static to cause the problem.

Suggestions for Incoming Test

The problem can be avoided by bringing up $\overline{CE}$ after Vcc has or by waiting 50 microseconds (the RECALL time specification) after the first time $\overline{CE}$ is brought low and then testing the SRAM again.

Note that bringing Vcc up with $\overline{CE}$ low and $\overline{WE}$ low (assuming $\overline{HBB}$ is high) will cause an SRAM write as soon as the part has completed its power-up RECALL; overwriting the SRAM after the power-up RECALL can be avoided by bringing $\overline{CE}$ high before Vcc is brought up.

Synopsis
It is possible to observe a false failure of STK1208 devices during incoming test if the Chip Enable ($\overline{CE}$) pin is brought high before power is applied to the device. While this does not harm the device or disrupt the nonvolatile data in any way, it will appear that the SRAM will not read/write correctly for the length of a RECALL cycle (approximately 15 microseconds at 5V at room temperature). The failure will only occur on the first SRAM test after the device arrives at the test location; after this first test, the part will function normally as long as it remains packaged.

Discussion

A node in an internal test mode control circuit connected to the address pin A0 can be pulled high by static charge when the part is handled just prior to incoming test. If the internal mode is high when the part is powered up with $\overline{CE}$ high, the first time $\overline{CE}$ is brought low, the part will perform a RECALL - disabling the SRAM, instead of appearing as though the part has failed the SRAM read or write. Bringing $\overline{CE}$ low disables the internal mode allowing the device to function normally.



Using the SIMTEK STK12C68 AutoStore™ 8K x 8 High Performance Nonvolatile Static RAM

Abstract

Simtek Corporation's STK12C68 is a fast static RAM backed by a nonvolatile EEPROM shadow memory in an industry standard 28 pin package. The SRAM portion of memory operates similarly to other 8Kx8 fast SRAM products and is easily interfaced to embedded processors and logic elements. The uniqueness of Simtek's nvSRAMs is their ability to *Store* data indefinitely without the need of batteries or other power sources while still operating at full processor speeds with no wait states. SRAM data can be *Stored* into nonvolatile memory under hardware or software control and is autonomously saved upon power-down. Data *Stored* in the EEPROM is automatically *Recalled* upon power-up without the need for processor intervention or the generation of external control signals. Data is *Stored* and *Recalled* in parallel, resulting in very fast nonvolatile operations (high bandwidth) that are ideally suited to a broad range of embedded processor and state machine applications.

Design, Packaging and Board Layout Considerations

The STK12C68 comes in three industry standard package styles: 300-mil DIP, 600-mil DIP, and 350-mil SOIC (Gull Wing). It is available in commercial and industrial temperature ranges in plastic packages, and in the military temperature range in ceramic. While the 12C68 pin-out for address, data, and control conforms to industry standard packaging for fast SRAM, it must be noted that the 12C68 has only one chip select rather than the normal two. This was done to accommodate the requirement for a control line to initiate and monitor hardware *Store* operations. The Hardware-Store-Busy pin (HSB) is a bi-directional control line that starts nonvolatile *Store* operations if taken low by external circuitry. This feature is locked out by internal logic if SRAM data hasn't changed since the last nonvolatile *Store* or *Recall*. HSB also serves as a "Store Operation Busy" monitor line that is internally driven low during all nonvolatile *Store* operations. HSB should be pulled to V_{CC} through a 10K Ohm resistor to help eliminate noise-induced *Store* operations and to assure a true logic high when not in an active condition (See Figure 1, for

example).

If the STK12C68 is being used to replace single chip select slow SRAM (BatRAM, etc.), PCB, circuitry, and logic changes are minimal. The addition of a 100 μ f capacitor from V_{CAP} (pin 1) to Gnd, and appropriate logic changes to handle Hardware *Store* Operations (pin 26), if desired, are all that is necessary to implement the full capabilities of the 12C68.

As with any high speed SRAM, a good quality (low inductance) decoupling capacitor is required from chip power to ground. Since the STK12C68's internal circuitry is powered from V_{CAP} , the decoupling capacitor must be connected from pin 1 to ground. Lead lengths should be kept short to minimize stray inductance and to provide a low Z path to ground for high frequency noise.

The STK12C68 also eases manufacturing and package layout problems associated with other manufacturers' nvRAMs. Its standard package dimensions (including height) allow the usage of automated pick and place machines and standard PCB layouts. Because it contains no batteries it can be flow soldered and eliminates the need for costly manual operations.

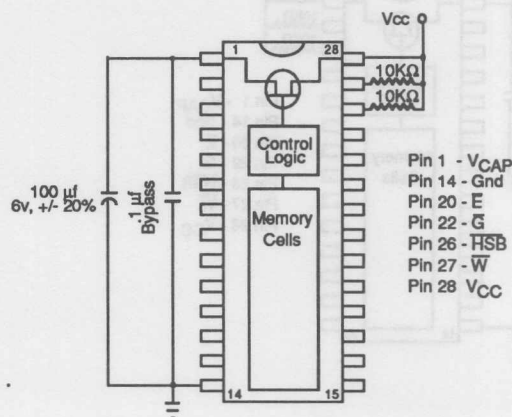


Figure 1
Typical STK12C68 Configuration

V_{CC} Connection Options

The STK12C68 can be connected to V_{CC} in one of three ways, depending on system characteristics and requirements. The most common connection, illustrated in Figure 1, involves the use of a 100μF capacitor on the V_{CAP} pin (pin 1). This connection scheme guarantees that an *AutoStore*[™] will occur on power-down (if the SRAM has been written), using the charge stored in the 100μF capacitor to complete the *Store* cycle. When V_{CC} drops below V_{SWITCH}, the STK12C68 disconnects itself from the system power bus and executes a *Store* cycle, saving the SRAM data to the EEPROM array.

Figure 2 shows a V_{CC} connection that still enables an *AutoStore*[™] when V_{CC} collapses, but requires that the system V_{CC} remain between V_{SWITCH}(minimum) and 3.5V for at least 10 milliseconds. In this case, a 100μF capacitor is not needed because the STK12C68 simply uses the system power to execute the *Store* cycle.

Figure 3 illustrates a connection that will prevent *AutoStores*[™] from ever occurring. By permanently grounding V_{CCX} (pin 28) and connecting system V_{CC} directly to V_{CAP} (pin 1), the internal power FET between pins 1 and 28 is held off and *AutoStores*[™] are disabled. In this configuration, the user can still initiate *Stores* through either address sequences or by pulling the *HSB* pin low.

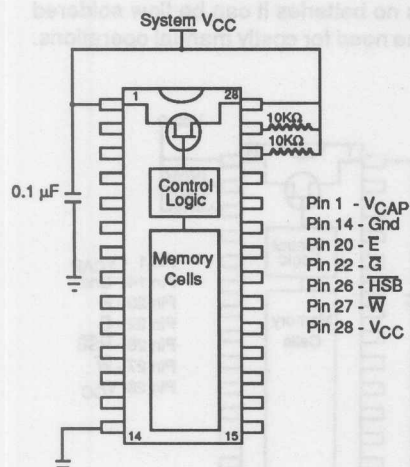


Figure 2
AutoStore[™] (relies on capacitor for *AutoStore*[™])

Note that it is not permissible to change between these three options "on the fly". Specifically, connecting up V_{CC} as shown in Figure 1 or 2 and then changing to the connection in Figure 3 is forbidden. If this is attempted, it is very likely that the device will be destroyed due to high current flow through the internal power FET which, under certain conditions, can effectively remain on for several seconds after power is removed from the part.

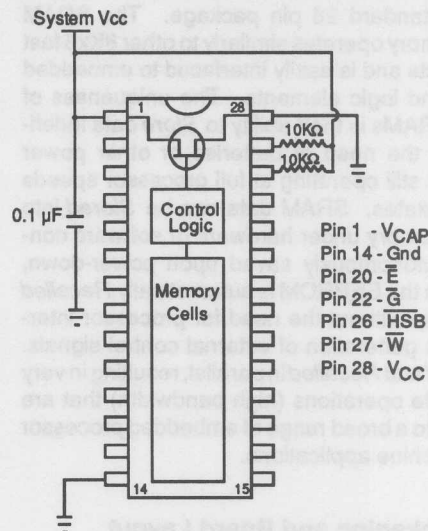


Figure 3
No *AutoStore*[™]

SRAM Operations

The STK12C68 8Kx8 high speed SRAM section operates similarly to other fast SRAMs on the market today. SRAM reads are performed whenever $\overline{E}$ and $\overline{G}$ are low, and $\overline{HSB}$ and $\overline{W}$ are high. The output data corresponds to the address specified on pins A₀₋₁₂.

A write to SRAM is performed whenever $\overline{E}$ and $\overline{W}$ are low, and $\overline{HSB}$ is high. The data on pins DQ₀₋₇ will be written into the memory cell corresponding to the address present on pins A₀₋₁₂. It is suggested that the control line $\overline{G}$ (output enable) be held high during the entire write cycle to avoid a brief data bus contention on the common I/O lines.

If the STK12C68 is being used as an SRAM replacement in an existing design, a PWB or control logic modification may be required to accommodate the single

chip select ($\overline{E}$), and the Hardware-Store-Busy ($\overline{HSB}$) pins.

Nonvolatile Recall Operations

Nonvolatile *Recall* operations can be initiated in two different ways: (1) Software, and (2) Automatic power-up recall.

1. Software Initiated Recall

A *Recall* of data from nonvolatile memory to SRAM is accomplished in a manner similar to the software *Store* operation. A series of six addresses are read to begin the *Recall*. The addresses must be read in the following order:

- (1) 0000H
- (2) 1555H
- (3) 0AAAH
- (4) 1FFFH
- (5) 10F0H
- (6) 0F0EH - *Recall* Operation Initiated

2. Power-Up Initiated Recall

The STK12C68 automatically *Recalls* the data *Stored* in nonvolatile memory upon power-up. Internal control logic initiates the *Recall* when system V_{CC} rises above V_{SWITCH} .

Nonvolatile Store Operations

Nonvolatile *Store* operations can be initiated in three different ways on the STK12C68: (1) Hardware, (2) Software, and (3) Automatic power-loss *Store* (*AutoStore*[™]).

1. Hardware Store

Hardware *Stores* can be initiated externally by pulling the $\overline{HSB}$ pin low for a minimum of 250ns. Internal circuitry will then keep the pin low for the duration of the *Store* operation. Care should be exercised to assure that $\overline{HSB}$ is not externally pulled high until after the *Store* has completed and the internal logic has released the pin. During hardware initiated *Stores* pins DQ₀₋₇ assume a high Z output condition and remain tri-stated until the operation completes (10ms maximum). Internal control logic prevents the 12C68 from performing additional Hardware *Store* operations if no SRAM write has taken place since the last *Store* or *Recall* cycle. This helps eliminate the chance of multiple *Store* operations during power-up or because of noise on the $\overline{HSB}$ pin.

Hardware-Store-Busy ($\overline{HSB}$) is a high speed, low drive

capability bi-directional control pin. It is important that $\overline{HSB}$ be pulled to system V_{CC} through a suitable pull-up resistor (10K Ohm typical) to assure that *Store* operations are not initiated by noise, or during bus direction transitions. The $\overline{HSB}$ pull-up resistor serves to lower the line impedance and helps to control induced noise that could initiate unexpected *Store* operations. Due to the low output drive capability of the $\overline{HSB}$ pin, it is important that the pull-up resistor value be selected carefully so as not to swamp the output driver (less than 3mA). While this will not cause damage to the chip, it could inhibit the STK12C68's automatic power loss *Store* capability (*AutoStore*[™]) and could result in inadvertent data loss.

2. Software Store

Data can also be *Stored* into the nonvolatile memory on the STK12C68 under software control. This process involves the reading of six addresses in sequence to begin the *Store*. It is important to assure that Read operations are performed instead of Writes or the cycle will not occur. Software *Store* takes place regardless of whether an SRAM Write took place since the last nonvolatile cycle. The address locations to be read are:

- (1) 0000H
- (2) 1555H
- (3) 0AAAH
- (4) 1FFFH
- (5) 10F0H
- (6) 0F0FH - *Store* Operation Initiated. $\overline{HSB}$ pin is active (low) for the duration of the *Store*.

3. Automatic Power-Loss Store (*AutoStore*[™])

If a 100 μ f capacitor is connected between V_{CAP} and Gnd, and if power is applied to V_{CCX} (pin 28, see *Figure 1*), the STK12C68 will automatically *Store* the SRAM data to nonvolatile memory upon sensing power loss. V_{CAP} is automatically disconnected from system V_{CCX} by an internal power FET when system power drops below V_{SWITCH} . Current is then drawn from the storage capacitor during the *Store* operation. This function is completely automatic and requires no external commands.

If the system power supply has sufficient output capacitance to assure that V_{CC} will not decay from V_{SWITCH} (minimum) to 3.5 volts in less than 10ms, the energy storage capacitor can be eliminated. With V_{CC} tied to both V_{CAP} and V_{CCX} (*Figure 2*) the STK12C68 will perform an *AutoStore*[™] every time V_{CC} drops below V_{SWITCH} , assuming an SRAM Write has taken place since the last nonvolatile cycle.

If automatic power down *Stores* are not required, the 100 μf energy storage capacitor can be eliminated (Figure 3). System V_{CC} is then tied directly to V_{CAP} and V_{CCX} is grounded. This will disable the *AutoStore™* function but will still allow nonvolatile *Stores* to be initiated via the HSB pin or under software control.

Low Power Operation

The STK12C68 is designed to use minimum power when the chip select pin, $\bar{E}$, is not selected. During this time the chip consumes only standby current. Total chip power dissipation during operation is determined by several factors, the most important of which is system access cycle time. The faster the memory is accessed, the higher the current requirements of the chip. Secondly, whether the chip is being driven at TTL or CMOS levels has an effect on total power requirements. At CMOS input signal levels the STK12C68 consumes less power than it does when driven with TTL gates. Other factors include V_{CC} voltage level and operating temperature.

The STK12C68 is designed to minimize power automatically by internally shutting down unnecessary cir-

cuitry during read operations. Approximately 55ns after $\bar{E}$ goes low, current will drop to standby level.

It can be seen from Figure 4 that the changes required to switch from the Dallas Semiconductor DS1225Y to the SIMTEK STK12C68 *AutoStore™* are minimal. The 100 μf *AutoStore™* capacitor may be eliminated if the system power decay time is >10ms between V_{SWITCH} (minimum) and 3.5 volts.

Conclusion

The Simtek STK12C68 is a high performance nonvolatile SRAM that is a perfect fit for applications requiring high speed, nonvolatile memory. Its ease of use makes it a natural choice where batteries and other nonstandard packaging concerns rule out other technologies. Its high speed allows it to operate where other technologies (BatRAM, Flash, EEPROM) can't, such as embedded DSP and other fast processor applications. Its long data retention times and high reliability make it a natural choice for users that require secure data retention, such as is found in the military, financial, and gaming industries.

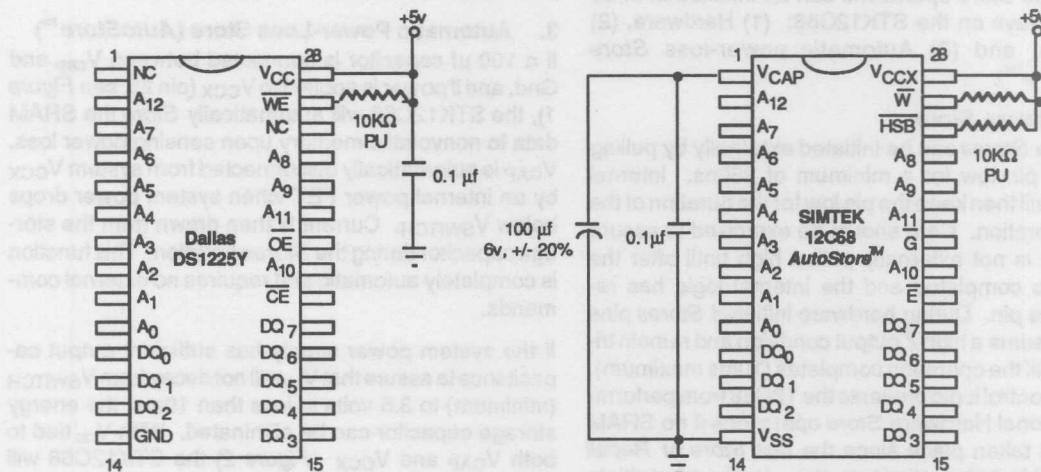


Figure 4
Comparison between Dallas DS1225Y and Simtek STK12C68



Applying the STK15C88 and STK11C88 32K x 8 nvSRAM

Abstract

Simtek Corporation's family of high speed 256 kilobit nonvolatile Static Random Access Memories includes the STK15C88 *AutoStore*TM and STK11C88 *Software Store* devices. Both memories have industry-standard 32K x 8 architectures and pin-outs (Figure 1), and are drop-in replacements for many standard SRAM and BatRAM products. As with all Simtek nvSRAM products, the STK11C88 and STK15C88 do not require batteries or other power sources to maintain nonvolatility for a guaranteed minimum of 10 years, even at high temperatures. The STK15C88 *AutoStore*TM memory automatically *Stores* data upon power loss, and requires no external power storage components such as batteries or capacitors. It is available in speeds of 25, 35, and 45 nanoseconds.

The STK11C88 *Software Store* memory is designed for safe storage of data under processor control. The STK11C88 virtually eliminates the danger of inadvertent data loss due to human error or electronics failure. It is ideally suited for applications that would normally require the combination of high speed SRAM and EEPROM, and performs both functions in one package. The resultant savings in board space, glue logic (parts count), and power consumption helps to reduce costs and increase packaging density. The STK11C88 is available in 25, 35, and 45 nanosecond versions, and can be interfaced to most standard microprocessors without interface logic or memory wait states.

Both memories automatically *Recall* nonvolatile data into the SRAM portion of the chip at power-up without processor intervention or external control. Simtek's family of nonvolatile memories give the product development engineer the ability to design modern embedded and state machines without the worry of data loss or corruption due to power failure.

STK11C88/STK15C88 SRAM Operations

The STK11C88 and STK15C88 nvSRAM memories are identical in the operation of their RAM front ends, and look to the design engineer like industry standard 32K x 8 fast SRAMs.

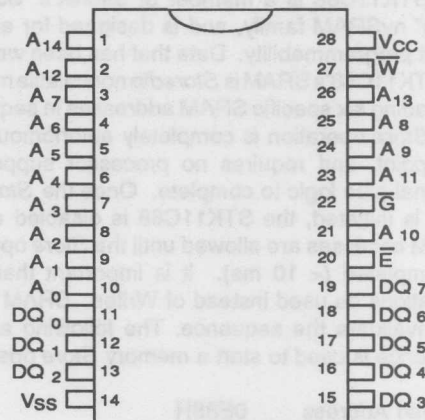


Figure 1
STK11C88/STK15C88 Pin-Out

The three control lines, Write Enable ($\overline{W}$), Chip Enable ($\overline{E}$), and Output Enable ($\overline{G}$) are utilized in the same manner as a standard SRAM. This front end functional equivalency allows improvements to be made to old designs without PWB (Printed Wiring Board) or control logic changes. The ability of Simtek's nvSRAM devices to run at processor bus speeds eliminates the need for wait states, bus control logic, or specialized decoder circuitry. This combination of speed and versatility in one package serves to simplify board layout and reduce device count.

SRAM *Reads* are performed whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The output data on lines DQ₀ - DQ₇ corresponds to the address specified on pins A₀ - A₁₄.

SRAM *Writes* are performed whenever $\overline{E}$ and $\overline{W}$ are low. The data on pins DQ₀ - DQ₇ will be written into memory at the location specified by the address present on lines A₀ - A₁₄. The $\overline{G}$ (Output Enable) line should preferably be held high during the entire Write cycle to avoid bus contention on the data lines.

The STK11C88 and STK15C88 are high speed memo-

Applying the STK11C88/STK15C88

ries and therefore must have a high frequency bypass capacitor of approximately 0.1 μ f connected between V_{CC} and Gnd. As with all high speed CMOS integrated circuits, careful routing of power, ground and signals will help to reduce noise induced problems.

STK11C88 Nonvolatile Operations

nvSRAM Store

The STK11C88 is a member of Simtek's "Software Store" nvSRAM family, and is designed for easy in-circuit programmability. Data that has been written to the STK11C88's SRAM is *Stored* to nonvolatile memory by reading six specific SRAM addresses in sequence. The *Store* operation is completely autonomous from that point, and requires no processor support nor external glue logic to complete. Once the *Store* process is initiated, the STK11C88 is disabled and no SRAM accesses are allowed until the *Store* operation is completed (< 10 ms). It is important that Read operations be used instead of Writes. SRAM Writes will invalidate the sequence. The following address sequence is used to start a memory *Store* operation:

1. Read Address 0E38H
2. Read Address 31C7H
3. Read Address 03E0H
4. Read Address 3C1FH
5. Read Address 303FH
6. Read Address 0FC0H (Initiate *Store* Cycle)

The chance of inadvertently reading the correct six addresses in sequence, and accidentally corrupting the data *Stored* in the STK11C88's nonvolatile section, is less than 1 chance in 10²⁵.

nvSRAM Recall

STK11C88 data is *Recalled* from nonvolatile memory to SRAM during power-up. A *Recall* is automatically initiated when internal circuitry senses V_{CC} levels rising above approximately 4.25 volts (V_{SWITCH}). Embedded processor wake-up sequences (power-on reset), should be delayed for a minimum of 550 μ s (t_{RESTORE}) after V_{SWITCH} to assure that data is completely *Recalled* and to allow the system to stabilize before attempting nvSRAM accesses.

Data can also be *Recalled* under software control in a manner similar to the *Store* operation. Six addresses are read in sequence to initiate the transfer from nonvolatile memory to SRAM. The following address sequence is used to start a memory *Recall*:

1. Read Address 0E38H

2. Read Address 31C7H
3. Read Address 03E0H
4. Read Address 3C1FH
5. Read Address 303FH
6. Read Address 0C63H (Initiate *Recall* Cycle)

It takes a maximum of 20 μ s for data that was *Stored* in nonvolatile memory to be *Recalled* to SRAM.

STK15C88 Nonvolatile Operations

The STK15C88 is very similar in operation to the STK11C88. Its software *Store* and *Recall* operations, and its power-up *Recall* capabilities are identical. The STK15C88 adds the capability of Simtek's *AutoStore*TM technology that allows it to sense power loss and *Store* data to nonvolatile memory autonomously without external circuitry or processor intervention. As with the STK11C88, once data is *Stored* into nonvolatile memory, no batteries, capacitors or external power sources are required to safely maintain the data for a minimum of 10 years. The only requirement for full *AutoStore*TM operation is that power supply voltage remain above 3.6 volts for a minimum of 10ms after Vswitch (approximately 4.25 volts, see Figure 2).

Even if the design engineer cannot guarantee the 10ms power supply voltage requirement, it is still possible to use the STK15C88 in many applications. The addition of a low forward voltage drop diode, and a 100 μ f capacitor will supply the energy necessary for the *Store* operation to complete independent of the Power Supply decay characteristics (Figure 3). Note that this alternate configuration effectively raises the V_{SWITCH} level by the diode drop V_f.

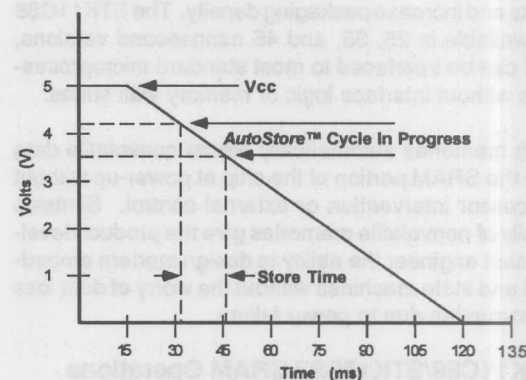


Figure 2

STK15C88 *AutoStore*TM Vcc Requirements

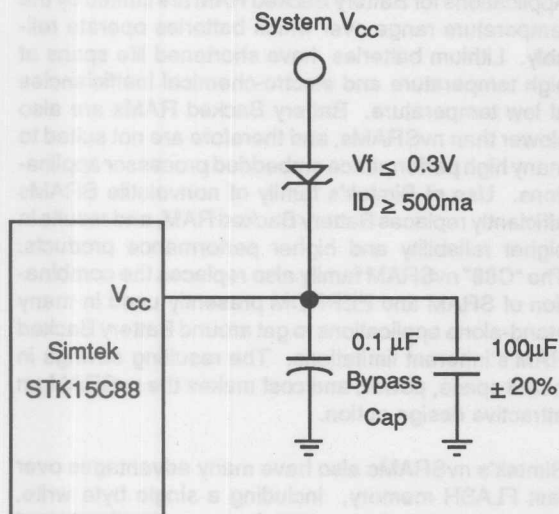


Figure 3
Alternate AutoStore™ Implementation

Applications

Simtek's family of nvSRAMs is the ideal complement to many of today's most advanced technologies. By increasing the level of integration, designs can be achieved that are smaller (more compact), lower in power, higher reliability, lower cost, and much higher performance than possible just a few years ago.

FPGA/PGA

Many manufacturers of programmable gate arrays require high speed nonvolatile memory to load configuration table data into their programmable arrays. Combining the high speed and density of Gate Array devices from Xilinx and Altera, with the advanced capability of the Simtek 32K x 8 family of nonvolatile memories, opens the door to many new embedded applications. Adaptive security systems, video/telecom Digi-Cypher, and automotive theft protection and recovery systems are just a few of the potential applications for embedded PGA/ nvSRAM systems (Figure 4).

By using a single STK11C88 nvSRAM to parallel load configuration data to an Altera EPLD, and by using the same memory as a fast SRAM for processor scratch pad RAM memory, the design engineer can realize a significant reduction in parts count and cost. At system power-up, the EPF81500 is held in a reset condition for

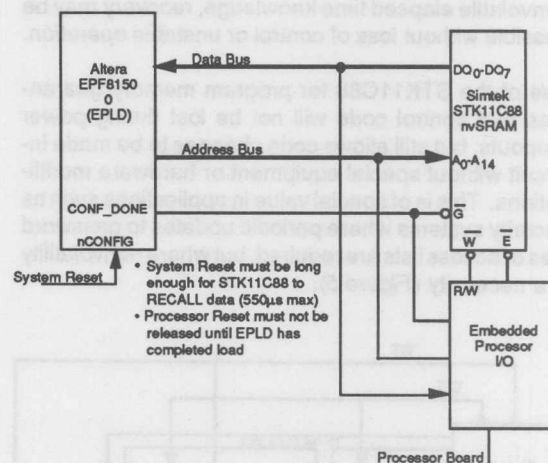


Figure 4
Altera EPF81500 EPLD in a parallel load
configuration with the SIMTEK STK11C88
256K "Fast" nvSRAM

a minimum of 550μs after Vcc reaches 4.1 volts. This allows sufficient time for the STK11C88 to Recall data from its nonvolatile memory into SRAM. After system reset is released the EPF81500 will request data from the STK11C88 (pull CONF_DONE line low) and begin sending addresses in a sequential count up or count down manner. After data is loaded into the EPLD, it will release the CONF_DONE line allowing the STK11C88 to be accessed by the embedded microprocessor. It is required that the microprocessor be held in reset until the EPF81500 is finished loading. This simple approach solves the problem of needing both fast SRAM scratch pad memory and nonvolatile memory to load the Altera device.

nvSRAM and TI-TMS320C52

Use of Simtek's 256K parts allows the TMS320C52 to run at its fully rated 80 megahertz with no wait-states. This design approach also assures that all calculated or measured control variables are saved in the event of power failure. No glue logic or interface components are required for systems of up to 96K words of nonvolatile memory, and only minimal external logic for systems of up to 192K words. This compact, efficient memory design simplifies PCB layout, improves system reliability, and reduces cost. Since memory data

is safe when power fails, short V_{CC} drop-outs will not necessarily result in loss of control or require system re-boot. If the on-board real-time clock maintains nonvolatile elapsed time knowledge, recovery may be possible without loss of control or unstable operation.

Use of the STK11C88 for program memory guarantees that control code will not be lost during power dropouts, but still allows code changes to be made in-circuit without special equipment or hardware modifications. This is of special value in applications such as security systems where periodic updates to password files or access lists are required, but where nonvolatility is a necessity (Figure 5).

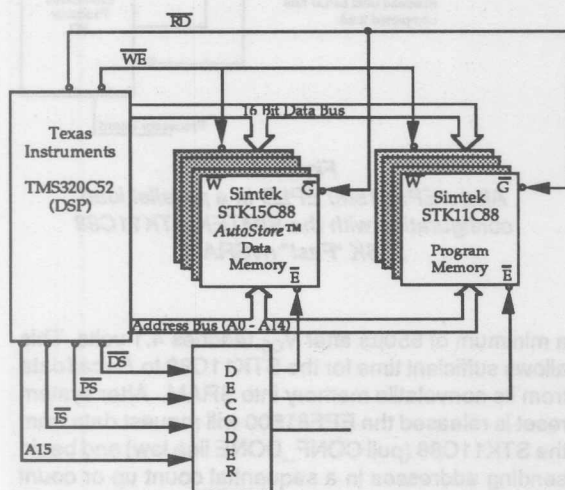


Figure 5

High Performance Embedded DSP System Using the TMS320C52 with the Simtek STK11C/15C88

Conclusion

Applications for Battery Backed RAM are limited by the temperature range over which batteries operate reliably. Lithium batteries have shortened life spans at high temperature and electro-chemical inefficiencies at low temperature. Battery Backed RAMs are also slower than nvSRAMs, and therefore are not suited to many high performance embedded processor applications. Use of Simtek's family of nonvolatile SRAMs efficiently replaces Battery Backed RAM, and results in higher reliability and higher performance products. The "C88" nvSRAM family also replaces the combination of SRAM and EEPROM presently used in many stand-alone applications to get around Battery Backed RAM's inherent limitations. The resulting savings in board space, power, and cost makes the nvSRAM an attractive design option.

Simtek's nvSRAMs also have many advantages over fast FLASH memory, including a single byte write, single operating voltage (5V), faster access times, and unlimited SRAM Write cycles. nvSRAMs also have the ability to perform Store operations autonomously without processor intervention or the requirement to run FLASH store algorithms. This results in less processor overhead, reduced parts count and higher product reliability.

The Simtek "C88" family of nonvolatile memories is fast, versatile, and cost effective for many types of modern high performance designs. The combination of speed and nonvolatility in one package allows high technology processing engines to operate at their full potential. The added advantage of remote programmability without the need to modify hardware, simplifies field upgrades and lengthens product lifetimes.



Using nvSRAM in RAID Controller Applications

Introduction

The term RAID (Redundant Array of Independent Disks) first appeared 5 years ago in papers written by Garth Gibson, Randy Katz, and Dave Patterson of the University of California at Berkeley. Since that time the number of manufacturers of RAID systems has expanded to over 100 companies with product lines that range from high end commercial products to lower cost controllers for the home market.

The RAID advisory board (RAB) was formed in 1992 to help minimize confusion within the industry by standardizing terminology and maintaining standards for the classification and typing of controllers. The board is comprised of over 40 members and continues to promote the industry by encouraging the development of hardware components that are optimized for RAID applications. The goal of the RAB is to become a compliance verification and testing organization that will issue product approvals, act as a regulatory agency, and assure users that the RAID level claimed by the manufacturer meets RAB standards. The RAB also will perform testing to certify that vendor hardware meets RAB requirements for Array-Ready Disks, and verify Disk Array Performance Benchmarks. The RAB is chaired by Joe Molina, President of Technology Forums - St. Peter, Minnesota 56082-9423 (507-931-0967).

RAID Theory Overview

For disk I/O intensive systems there are two characteristics that act as the primary system performance bottlenecks:

1. Data Seek Time
2. I/O Transfer Rates

It would seem logical that all that is required to reduce the time necessary for the computer to fetch data from the disk is to use multiple disks in parallel and distribute the data. While this solution sounds easy and cheap, the realities of life aren't so simple. As any experienced

system administrator can tell you 80% of the total I/O load of a system is directed at 20% of the I/O resources. This so-called 80/20 rule requires that the I/O system be tuned to distribute the load over the bank of parallel disks. This evens out the number of I/O requests per disk and greatly speeds up the disk access. The trouble with disk tuning is that it requires a lot of system administration time to accomplish, and when done, there is no guarantee that it will stay balanced. In a dynamic system the I/O load will change with time and therefore will require constant tweaking to maintain peak efficiency. A better solution is to use an array of disks. The RAB defines an array of disks as "a collection of disks from one or more commonly accessible disk subsystems, combined with a body of Array Management Software (AMS)".

Array Management Software is usually defined as firmware that executes in a dedicated control system rather than the host computer and has two major functions. Function one is to map the storage space available and optimize system balance to maximize disk I/O performance. Function two is to present storage to the operating environment as virtual disks by converting I/O requests to virtual disk I/O requests. This gives the appearance of a single large disk to the system and frees the administrator from constantly having to tweak the data distribution. Disk arrays generally have improved I/O performance, and simpler storage management requirements than a string of parallel disks.

The next task facing the designer of RAID systems is to assure that data stored in the array can never be lost due to hardware failure. Major users of disk array systems such as banks, airlines, and credit agencies must be certain that they can never lose a disk in such a manner that the data stored on that disk is not recoverable. Even frequent and conscientious backing up of all disk storage does not recover new data that has been written since the last backup cycle was performed. A solution to this data reliability problem is the use of a RAID Controller. RAID Controllers are

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defined with 7 levels:

Level 0 - Data Striping

Level 1 - Disk Mirroring

Level 2 - Hamming Code

Level 3 - Parallel Transfer Disks with Parity

Level 4 - Independent Access Array

Level 5 - Independent Access Array with Rotating Parity

Level 6 - Recovery from the failure of up to 2 disks

RAID Level 0

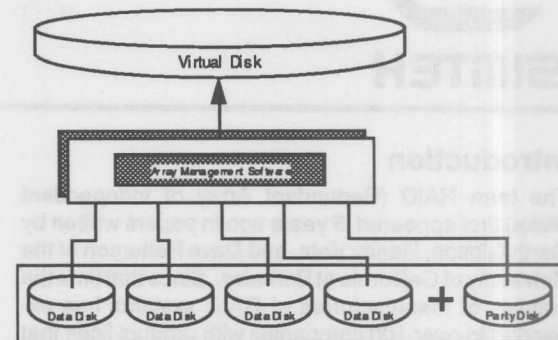
A stripe set presents a single virtual disk whose capacity is equal to the sum of the capacities of its members. The reliability of the stripe is less than the reliability of its least reliable member and its read and write rates are high. RAID 0 is not a true RAID controller because it provides no redundancy. It is, however, a performance-oriented architecture that is inexpensive and therefore attractive to many low cost users. RAID 0 is a parallel transfer technology.

RAID Level 1

A mirror set also presents a single virtual disk; its capacity however is equal to that of its smallest member. Its reliability is very high, its read performance is usually better than that of a single member, but its write performance is somewhat slower. A RAID 1 system protects against disk failure by replicating all stored data at least once on a physically separate disk. RAID 1 can be implemented as either a parallel or independent array and is well suited to applications that are read intensive and where reliability requirements are high.

RAID Level 2

A parallel access array that uses Hamming Coding to provide error detection and correction capability to the array. This approach is very expensive and therefore almost never implemented into a system.



*Example of a Typical RAID Level 3 or 4 Controller
From The RAIDBook Edition 1-1*

RAID Level 3

RAID 3 is optimized for high data transfer rates and is a parallel transfer technique with parity. Each data sector is subdivided, and data is scattered across all data disks with redundant data being stored on a dedicated parity disk. Reliability is much higher than a single disk and the data transfer capacity is the highest of all listed RAID types. RAID 3's weakness lies in its relatively slow I/O rates that make it unsuitable for most transaction processing unless assisted by some other technology such as cache. The parity disk stores redundant information about the data chunks stored in corresponding locations on the data disks. The redundant information is typically in the form of a bit-by-bit Exclusive OR function of corresponding data chunks from the other disks. Typical applications for RAID 3 include large data objects such as CAD files, graphical images, seismic or telemetered data streams.

RAID Level 4

RAID level 4 is an independent access array in which data sectors are distributed in a similar manner to disk striping systems. Redundant data is stored on an independent parity disk (similar to RAID 3). Its data reliability is much higher than a single disk (comparable to RAID 2, 3, and 5) and its data transfer capacity is moderate. RAID 4 is a high I/O read rate technology with moderate write speeds, but is not well suited for high data transfer applications due to the parity disk write bottleneck. Two of the four operations required to

perform a virtual disk write are directed at the parity disk; for this reason RAID 4 arrays are seldom implemented. Possible applications would include systems that are read intensive and do not require high data transfer rates.

RAID Level 5

RAID level 5 is an independent access array with rotating parity. Data sectors are distributed in the same manner as disk striping systems but redundant information is interspersed with user data across multiple array members rather than stored on a single parity disk as in RAID 3/4 systems. This relieves the write bottleneck associated with RAID level 4 controllers. RAID 5 arrays have high data reliability, good data transfer rates and high I/O rate capability. It is well suited to applications such as on-line customer services, inquiry-type transaction processing, group of office automation, etc.

RAID Level 6

RAID 6 is a non-Berkeley level controller that is designed for extremely high data reliability. RAID 6 is an independent access array concept that requires two parity blocks be updated for each block written. This

requires an extra parity disk but gives the added data safety of requiring 3 disks to fail before data will be lost. RAID 6 data transfer and I/O capability is lower than RAID 5 for writes, but data reliability is highest of all RAID architectures. Presently RAID level 6 is not widely used because of the higher costs associated with the added complexity, and the high penalty paid in system I/O performance due to long write times.

Additional RAID Implementations

RAID 10 is a combination of RAID 0&1. This architecture gives high I/O performance and good data reliability. It is accomplished by using RAID 0 (data striping) to enhance I/O rates and by using RAID 1 (disk mirroring) for high data reliability. RAID 10 requires costly hardware (disk and port) to implement, and is primarily used in applications where the data has high value and can justify a mirrored storage system.

RAID 53 is a combination of RAID levels 0 & 3 and provides RAID 3-like data transfer performance, and striping-like I/O request rates at RAID 3 or 5 costs. RAID 53 is used where both high data request rates and high data transfer performance is required such as airline reservation systems, financial and banking ap-

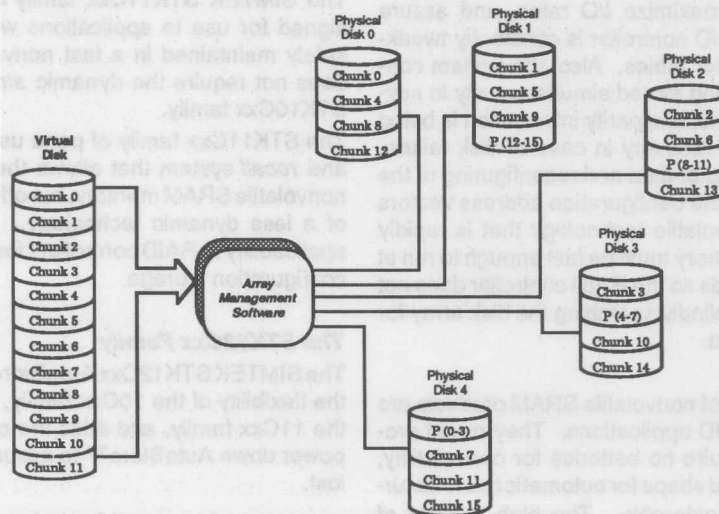


Figure 2
Example of a Typical RAID Level 5 Controller
From The RAIDBook Edition 1-1

plications, etc.

nvSRAM Applications and System Architecture

In modern RAID systems the Array Management Software can run in the host or in a dedicated embedded controller. Most modern systems are using embedded controllers with many manufacturers using the Intel i960 chip as the engine.

In the past RAID systems were designed to use a distributed block of disk to maintain system configuration and to store system recovery address vectors. The primary problem with this type of architecture is that if a power failure occurs, and the controller's volatile system memory is lost, the entire disk array must be scanned upon power up to reestablish configuration and to redefine data locations. On a large array this is very time consuming, requiring many minutes to accomplish. Service-oriented industries cannot afford this length of down time and must come up and be operating very quickly once power is restored. In the latest generation of RAID systems the restart vectors are stored in nonvolatile semiconductor memory on the controller board itself. Due to the fact that the Array Management System is constantly moving data among the individual array members to optimize I/O balance, maximize I/O rates, and assure redundancy, the RAID controller is constantly tweaking the address vector tables. Also, the system configuration data is being stored simultaneously in several different locations, and parity information is being maintained to allow recovery in case of disk failure. This constant moving of data and reconfiguring of the array, requires that the configuration address vectors be stored in a nonvolatile technology that is rapidly rewritable. This memory must be fast enough to run at processor bus speeds so the RAID controller does not have to waste time blindly searching the disk array for its configuration data.

The SIMTEK family of nonvolatile SRAM products are ideally suited to RAID applications. They run at processor speeds, require no batteries for nonvolatility, are standard size and shape for automatic manufacturing, and are flow solderable. The high number of nonvolatile stores (100K), fast read and write times (25 nsec), and fast store times (10 ms) allows the design

of highly efficient embedded controllers for both commercial and home applications.

Applying SIMTEK nvSRAM To Modern RAID Controllers

The STK10Cxx Family

The SIMTEK STK10Cxx family of nvSRAMs is a high performance nonvolatile memory family that is designed for easy interface to embedded controllers. The STK10Cxx family is designed for dynamic applications that require easy transfer from SRAM to nonvolatile memory under processor control. Using the 10Cxx family for *store* and *recall* of address vectors, configuration databases, and error detection/correction codes is an ideal application.

Data within the SRAM is stored to nonvolatile memory by simply requesting an SRAM write with the NE line active. This transfers data from the SRAM to shadow EEPROM in 10 msec. Data in the EEPROM is then completely nonvolatile and requires no batteries, capacitors or other energy sources to remain stored for 10 years.

The STK11Cxx Family

The SIMTEK STK11Cxx family of nvSRAMs is designed for use in applications where data must be safely maintained in a fast nonvolatile memory, but does not require the dynamic *store* capability of the STK10Cxx family.

The STK11Cxx family of parts uses a software *store* and *recall* system that allows the flexibility of a fast nonvolatile SRAM memory, but offers the data security of a less dynamic technology. This part has high applicability to RAID controllers for address vector and configuration storage.

The STK12Cxx Family

The SIMTEK STK12Cxx AutoStore™ family combines the flexibility of the 10Cxx family, the data security of the 11Cxx family, and adds the capability to perform power down AutoStore™ to assure that data is never lost.

The 12Cxx family uses the same *store* and *recall* techniques that are used with the 10/11C parts, but

also gives the design engineer the flexibility of automatically storing on power down. AutoStores™ are autonomously performed (unless inhibited) when system power falls below 4.2 volts. This assures that data is always safe and requires no batteries or other power sources that are prone to failure. RAID controllers that are dynamically keeping track of address vectors, system configuration, and disk error recovery information are ideal applications for this family of parts.

Conclusion

Modern RAID Controllers offer high data reliability and increased I/O performance in one package. This requires that the RAID system designer utilize the latest in high performance embedded processors,

state-of-the-art software, and sophisticated control algorithms.

The flexibility of fast nonvolatile memory for the storage of RAID address vectors, system configuration information, and adaptive algorithm memory is becoming more apparent with each new generation of system. SIMTEK's family of fast nvSRAMs are ideally suited to this type of high performance application. They run at processor speeds with no wait states, reliably store data in a nonvolatile semiconductor memory without batteries, and look to the processor like a standard SRAM. Ease of implementation and ability to rapidly change data, as well as the ability to use modern manufacturing techniques, helps to reduce costs and to speed product to market.

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also gives the design engineer the flexibility of automatically starting on power down. AutoSleep™ and wake modes are performed (when enabled) when system voltage falls below 4.2 volts. This assures that data is not lost and requires no batteries or other power source that are prone to failure. RAID controllers that are cyclically keeping track of address vectors, system configuration, and disk error recovery information are ideal applications for this family of parts.

Conclusion

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Using Simtek nvSRAMs with the Motorola DSP56002

The Motorola DSP56002 is a 24 bit, high-performance Digital Signal Processor that is ideally suited for audio, instrumentation, and automotive applications. When coupled with nonvolatile Simtek Static Random Access Memories (nvSRAM), the DSP56002 running at 40 Megahertz becomes a compact, cost-effective processing engine for a wide variety of OEM applications.

The DSP56002's external memory space is divided into Data Memory and Program Memory. Data Memory is further segmented into X Data Memory, and Y Data Memory. This allows the addressing of 192K words of memory with a 16 bit address bus. When Data Memory is made up of STK12/15CXX (Simtek AutoStore™ nvSRAM) components and Program Memory is made up of STK11CXX (Simtek Software Initiated Store nvSRAM), the DSP56002 becomes a complete processing engine capable of running at 40 Megahertz with no wait-states. The Simtek parts interface to the

DSP56002 with no glue logic and offer full nonvolatility without requiring batteries or processor intervention (Figure 1).

Data Memory

Using the STK12/15CXX AutoStore™ nvSRAM for Data Memory (Figure 2) guarantees that adaptive control data, calculated filter coefficients, and self calibration error correction tables will not be lost during power loss. Use of the STK12/15C88 family also allows the DSP56002 processor to run at a full 40 Megahertz rate with no wait states and without the requirement for special interface circuitry or glue logic.

The STK12/15CXX AutoStore™ Family

Simtek's STK12/15CXX family combines the speed of an EPROM, the flexibility of an EEPROM, and the

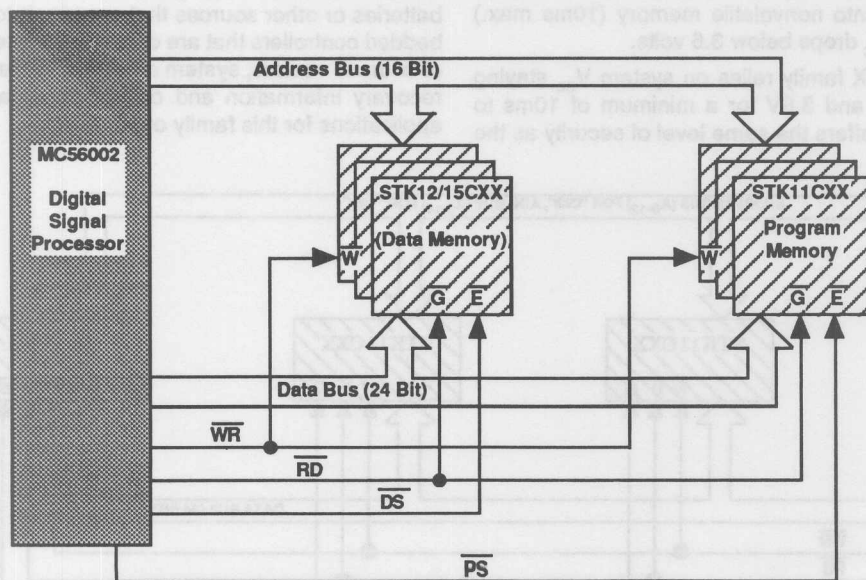


Figure 1
DSP56002 Digital Signal Processor and Simtek nvSRAM Block Diagram

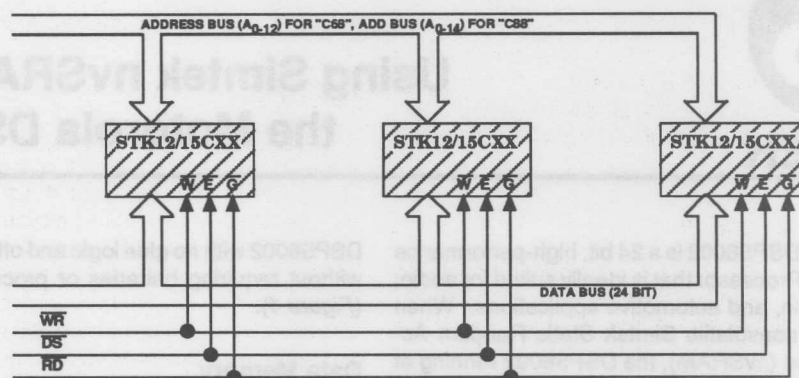


Figure 2
DSP56002 Data Memory Block Diagram

power loss data security of a battery-backed SRAM.

The STK12CXX and STK15CXX are functionally equivalent parts that offer the design engineer options for high performance Data Storage memory. The STK12CXX design uses an external energy storage capacitor (V_{CAP}) and incorporates an internal power switch that automatically isolates V_{CAP} from system power when V_{CC} drops below approximately 4.2 volts. V_{CAP} ensures that the SRAM data will have time to be safely *Stored* into nonvolatile memory (10ms max.) before chip V_{CC} drops below 3.6 volts.

The STK15CXX family relies on system V_{CC} staying between 4.2V and 3.6V for a minimum of 10ms to complete and offers the same level of security as the

STK12CXX family once data is *Stored*.

The STK12/15CXX family uses a combination of hardware *Store*, software *Store* and *AutoStore*™ capabilities to give the design engineer the flexibility and data security required for high-performance embedded control system applications. *AutoStore*™ operations are autonomously performed (unless inhibited) when system power falls below 4.2 volts. This assures that data is safe from inadvertent power loss and requires no batteries or other sources that are prone to fail. Embedded controllers that are dynamically keeping track of address vectors, system configuration tables, error recovery information and calibration data are ideal applications for this family of parts.

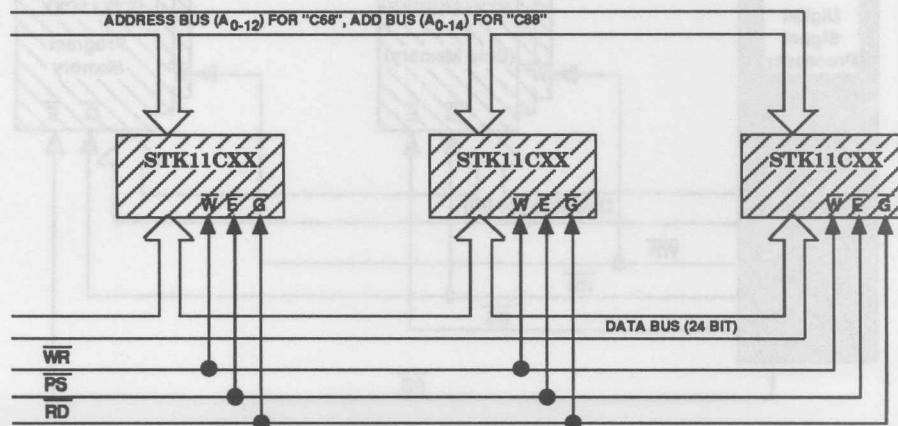


Figure 3
DSP56002 Program Memory Block Diagram

Program Memory

Using STK11CXX "Software Store" memory parts for program data (*Figure 3*) ensures that the processor embedded software cannot be inadvertently corrupted, while still allowing the flexibility of easy code changes and updates.

The STK11Cxx Family

Simtek's STK11Cxx family of nvSRAMs is designed for use in applications where data must be safely maintained in a fast nonvolatile memory, but do not require the *AutoStore*™ capability of the STK12Cxx family.

The STK11Cxx family of parts uses a software *Store* and *Recall* system that allows the flexibility of a fast nonvolatile SRAM memory, but offers the data security of a less dynamic technology. This part has high applicability to embedded controllers for program memory storage. The STK11Cxx can run at DSP56002 processor speeds with no wait-states, yet still allows the flexibility of in-circuit code changes without the

requirement for costly manual operations.

Conclusion

When the Motorola DSP56002 is teamed with Simtek's family of nonvolatile memory components, the resulting system is as safe as if it was using PROM for program memory, as fast as a system using SRAM for data memory without the danger of data loss, and as flexible as a system using EEPROM or battery-backed SRAM without the limitations associated with either. Critical control system or adaptive coefficient data is safe during unexpected or planned power outages, without the need for batteries or other exotic power sources. The program data is safely stored but maintains the flexibility to allow modification of the runtime code without changing components, or returning the hardware to the vendor.

Simtek's parts replace the combination of EEPROM and SRAM typically used in embedded applications resulting in a savings of board space, power, and cost.

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Program Memory

Using STK11CXX Software Store memory parts for program data (Figure 2) ensures that the processor will not be affected by any code changes while still allowing the flexibility of easy code changes and updates.

The STK11Cxx Family

Simtek's STK11Cxx family of nonVRAMs is designed for use in applications where data must be safely maintained in a fast nonvolatile memory, but do not require the "endless" capacity of the STK11Cxx family.

The STK11Cxx family of parts uses a software Store and a local system that allows the flexibility of a fast nonvolatile SRAM memory, but offers the data security of a non-volatile technology. This part has high capability to embedded controllers for program memory storage. The STK11Cxx family has 256Kb of memory storage with no wait states, yet still allows the flexibility of in-circuit code changes without the



Using the TMS320C52 DSP with Simtek's 32K x 8 nvSRAM (STK11C88/STK15C88)

The Texas Instrument TMS320C52 Digital Signal Processor

Texas Instruments' TMS320C52 is a fifth generation, enhanced member of the TMS320 line of Digital Signal Processors. Its modular architecture is optimized for ease of use, cost-effectiveness, and rapid development cycles. Its enhanced TMS320 instruction set is designed for fast algorithm development and high-level language operation. New static CMOS design techniques have minimized power consumption and maximized radiation hardness resulting in a powerful embedded compute engine for modern design.

The TMS320C52 is available in three speeds (40, 57, and 80 MHz) and is capable of more than 28 MIPS. The TMS320C52 is complete with 1 KWord of on-chip RAM and 4 KWords of on-chip ROM. It has two serial ports and is capable of accessing 64K parallel I/O ports. The TMS320C52 independently addresses Program and Data memory space of 64K words each. This modern dual memory configuration gives the "C52" increased performance and versatility, and allows full speed execution without the need for wait states or idle time. The Advanced Harvard Architectural design permits instant access to program memory and makes available intermediate computed values, such as adaptive coefficients, calibration, error correction tables and configuration information at full bus speeds. This state-of-the-art pipe-lined architecture also optimizes the "C52" for high speed throughput, and allows many executables such as multiply/accumulate operations to execute in a single machine cycle. The TMS320C52 emphasizes overall speed and flexibility in its configuration, and includes floating-point operations, block memory transfers, and multi-processing implementations.

Simtek's 256K nvSRAMs

Simtek Corporation has been manufacturing nonvolatile SRAM (nvSRAM) memories since 1989 and has recently expanded its product line to include the STK11C88 Software Store, and STK15C88 AutoStore™ memories. Simtek's 256K family of nvSRAMs is the highest density, fastest memory presently manufactured by Simtek. Simtek's SNOS process guarantees 10 year data retention without requir-

ing batteries, capacitors, or other energy sources.

The STK11C88

The STK11C88 is a 256 kilobit nonvolatile memory organized in a standard 32K x 8 SRAM architecture. The STK11C88 operates as a standard Static RAM and is available in 25ns, 35ns, and 45ns speed ratings. The STK11C88 is compatible with most Micro and Digital Signal Processors on the market, and is ideal for applications where battery backed RAM (batRAM) is unsuited (temperature, environmental, etc.), or where other technologies such as FLASH or EEPROM do not meet performance requirements. Data written into SRAM is *Stored* to nonvolatile memory by simply reading 6 addresses in sequence. This simple process initiates a nonvolatile *Store* operation that is complete in a maximum of 10ms. By using memory read operations instead of memory writes, no SRAM cells are corrupted and lost to the design engineer. The use of this memory control scheme results in a probability of accidentally corrupting *Stored* data is less than 1 chance in 10^{25} . A further advantage of the Software Store architecture is that no PWB or hardware design changes are required to switch from a standard SRAM memory to a nonvolatile STK11C88.

Data is automatically *Recalled* from nonvolatile memory to SRAM when V_{CC} rises above approximately 4.25 volts. Internal circuitry initiates the *Recall* and no processor intervention or outside control is required. Processor (software) initiated *Recall* of data from nonvolatile memory is accomplished by reading six addresses in sequence, similar to the *Store* initiation process.

The STK15C88 AutoStore™ Memory

The STK15C88 AutoStore™ Memory combines the Software Store capability of the STK11C88 and the power loss security of advanced Simtek AutoStore™ technology. The STK15C88 senses power loss at approximately 4.25 volts and automatically initiates a nonvolatile Store to save the data contained in its SRAM. AutoStore™ takes a maximum of 10ms and is totally automatic, requiring no processor or operator intervention and needs no external circuitry to complete. The only requirement for full AutoStore™ func-

Using the TMS320C52 with Simtek nvSRAMs

tionality is that the power supply voltage stay above 3.6 volts for at least 10ms after the start of the *Store* operation (See Figure 1).

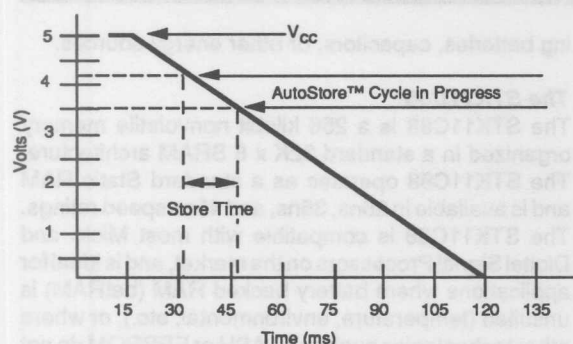


Figure 1
STK15C88 AutoStore™ Vcc Requirements

Once data is *Stored* into nonvolatile memory it is safe from loss for a minimum of 10 years even at high temperatures, and is *Recalled* automatically upon power recovery.

Software *Store* operations on the STK15C88 are identical to the STK11C88 and provide the same level of security and code protection.

Example System

Combining the TMS320C52 and Simtek's STK11C88 and STK15C88 memories makes a compact, robust embedded machine for high performance applications (See Figure 2).

Use of Simtek's family of 256K parts allows the TMS320C52 to run at its full rated 80 megahertz with no wait states. This design approach also assures that all calculated or measured control variables are saved in the event of power failure. No glue logic or interface components are required for systems of up to 96K words of nonvolatile memory, and only minimal external logic for systems of up to 192K words. This compact, efficient memory design simplifies PCB layout, improves system reliability, and reduces cost. Since memory data is safe when power fails, short V_{CC} drop-outs will not necessarily result in loss of control or require system re-boot. If the on-board real-time clock maintains nonvolatile elapsed time knowledge, recovery may be possible without loss of control or unstable operation.

Use of the STK11C88 for program memory guarantees that control code will not be lost during power dropouts, while still allowing code changes to be made in circuit without special equipment or hardware modifications. This is of special value in applications such as security systems where periodic updates to password files or access lists are required, but where nonvolatility is a necessity.

Conclusion

Combining the Texas Instruments TMS320C52 Digital Signal Processor and the Simtek family of nonvolatile Static RAMs opens performance doors for the systems designer that were previously closed. The combination of high speed and nonvolatility allows modern high performance processing engines to operate at their full potential. It also opens the way for innovative new applications and approaches to embedded controls. The elimination of batteries and capacitors helps to lower system and field maintenance costs, and solves many operating environment problems. The "C88" family, due to its high speed capability, reduces parts count by replacing the combination of SRAM and EEPROM presently used in many stand-alone applications. This results in more compact, lower power, and lower cost designs. The ability to change program code remotely without modifying hardware also allows remote field upgrades and lengthens product lifetimes.

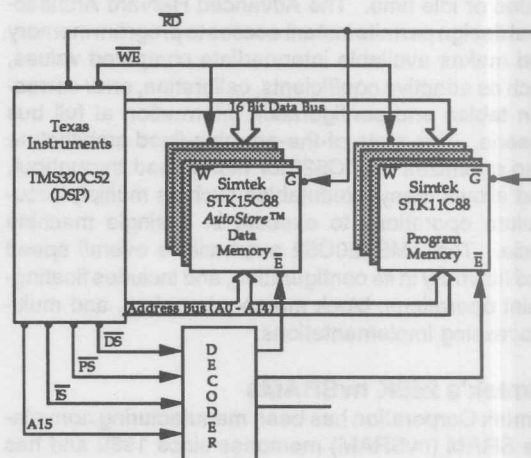


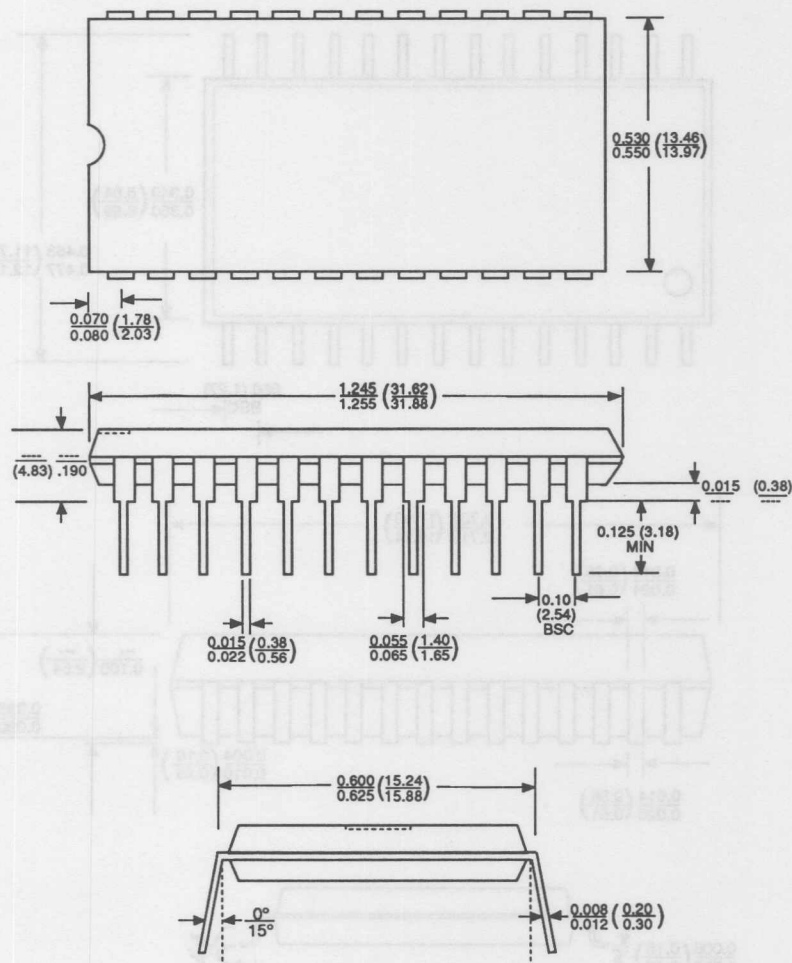
Figure 2
TMS320C52 and Simtek STK11C88 and
STK15C88 nvSRAMs
Embedded Processing System

Package Drawings 7



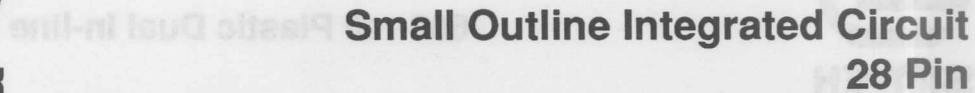
600-mil Plastic Dual In-line Package 24 pin

24 - 600 PDIP

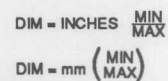


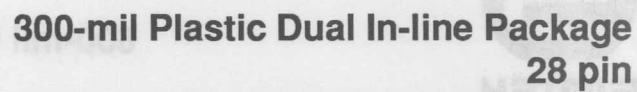
DIM = INCHES $\frac{MIN}{MAX}$

DIM = mm $\left(\frac{MIN}{MAX}\right)$



28 - SOIC





Technical drawing of a 16-pin D-subminiature connector. The drawing includes three views: a top view, a side view, and a front view. The top view shows a rectangular connector with a notch on the left side. The side view shows the profile of the connector with dimensions for height and width. The front view shows the 16 pins with dimensions for pin pitch, pin width, and pin height. Dimensions are given in inches and millimeters.

Top View Dimensions:

- Overall width: $.275$ (6.98) / $.295$ (7.49)
- Notch width: $.020$ (0.51) / $.030$ (0.76)

Side View Dimensions:

- Overall height: 1.345 (34.16) / 1.385 (35.18)
- Pin height: $.015$ (0.38)
- Pin pitch: $.125$ (3.18) MIN

Front View Dimensions:

- Pin pitch: $.100$ (2.54) BSC
- Pin width: $.030$ (0.76) / $.045$ (1.14)
- Pin height: $.014$ (0.36) / $.022$ (0.56)
- Pin width: $.045$ (1.14) / $.060$ (1.52)

Bottom View Dimensions:

- Overall width: $.300$ (7.62) / $.325$ (8.26)
- Pin pitch: $.008$ (0.20) / $.015$ (0.38)
- Pin height: $.008$ (0.20) / $.015$ (0.38)
- Pin pitch: $.300$ (7.62) BSC
- Pin height: $.430$ (10.92)

Notes:

- DIM = INCHES
- MIN / MAX

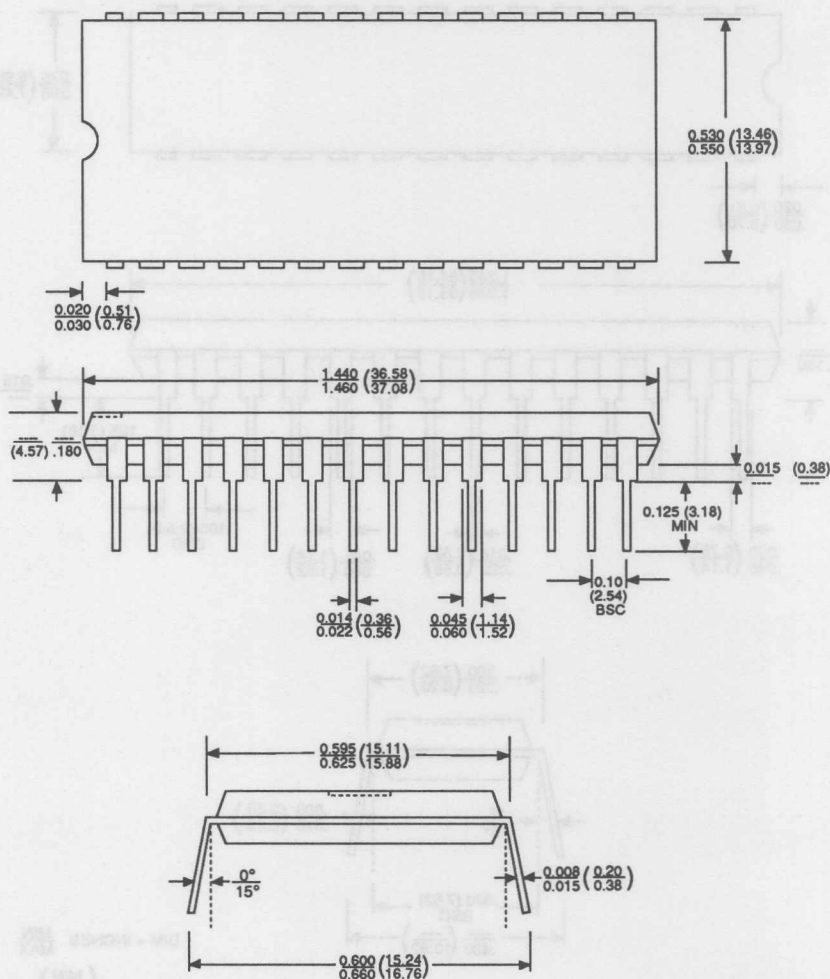
DIM - INCHES $\frac{\text{MIN}}{\text{MAX}}$

DIM = mm $\left(\frac{\text{MIN}}{\text{MAX}} \right)$



600-mil Plastic Dual In-line Package 28 pin

28 - 600 PDIP



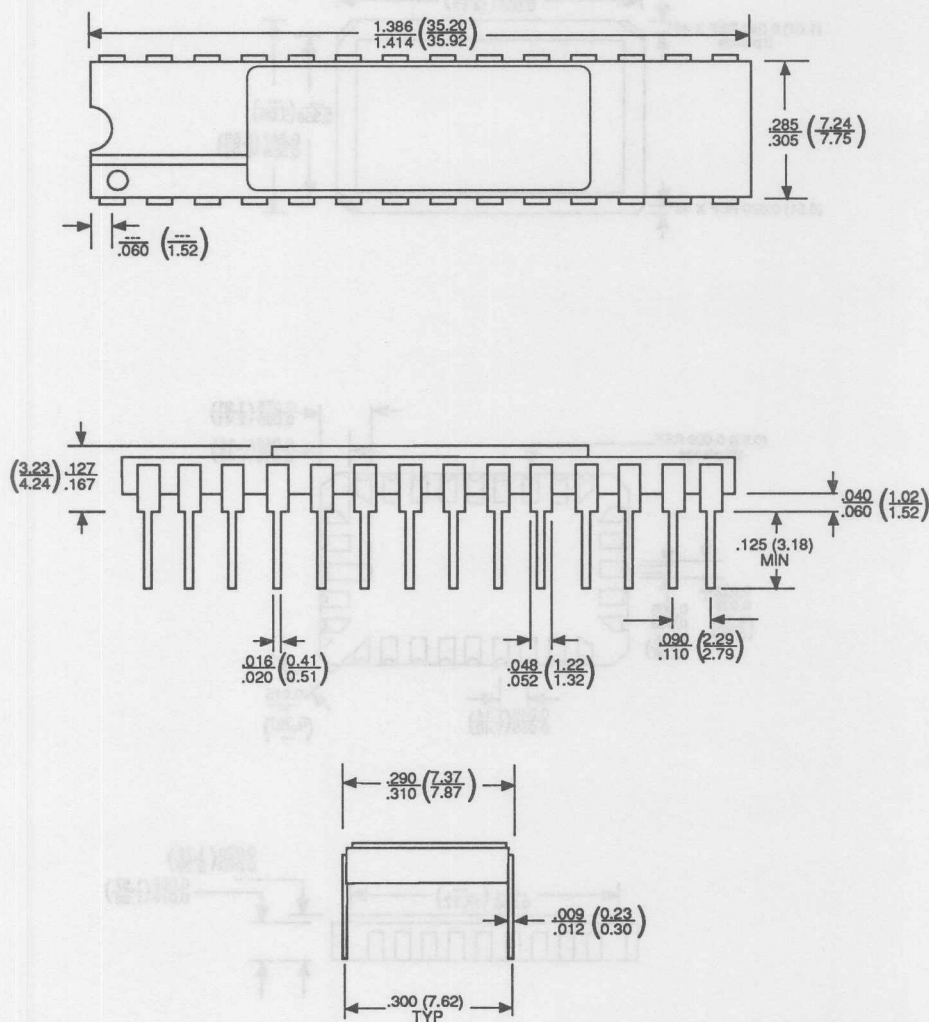
DIM = INCHES $\frac{\text{MIN}}{\text{MAX}}$

DIM = mm $\left(\frac{\text{MIN}}{\text{MAX}} \right)$



300-mil Ceramic Dual In-line Package 28 pin

28 - 300 CDIP



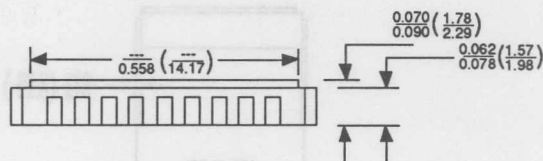
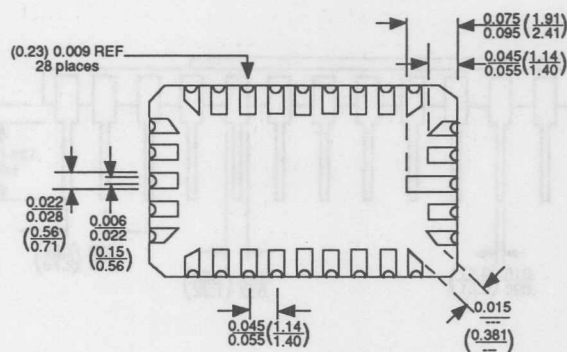
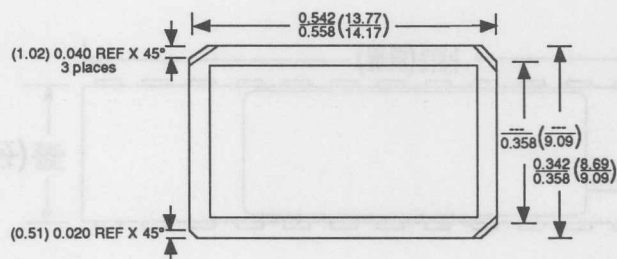
DIM = INCHES MIN MAX

DIM = mm (MIN MAX)



Leadless Chip Carrier

28 - LCC

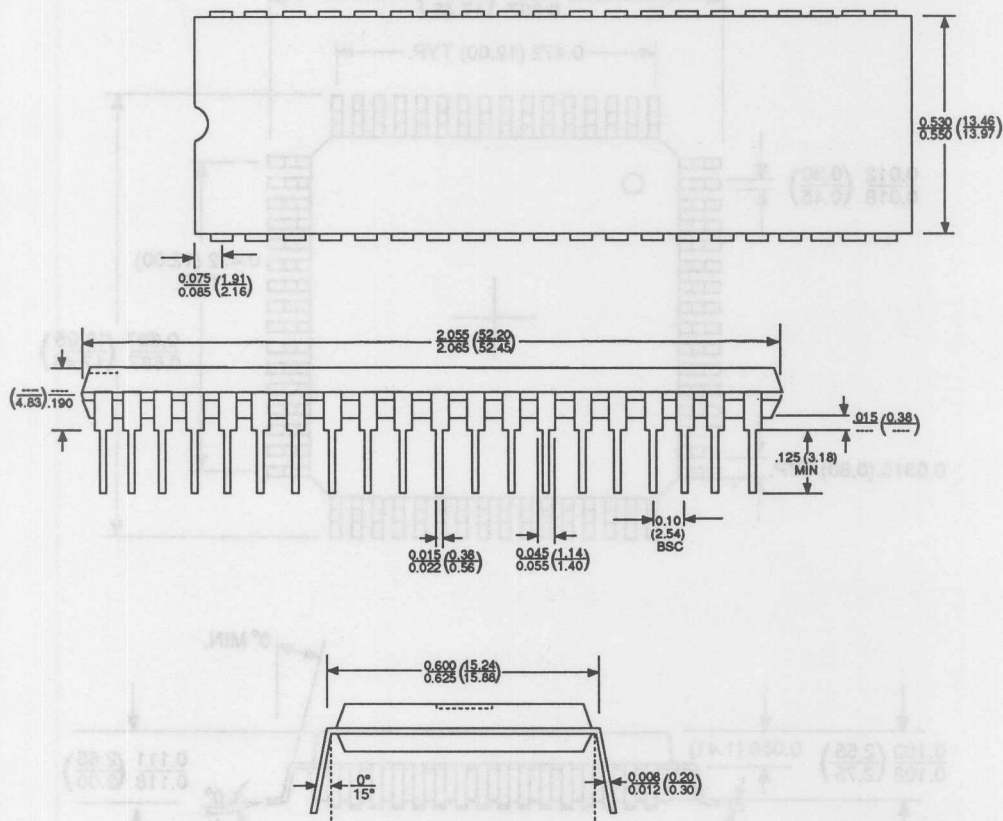


DIM = INCHES $\frac{\text{MIN}}{\text{MAX}}$
 DIM = mm (MIN) (MAX)



600-mil Plastic Dual In-line Package 40 pin

40 - 600 PDIP

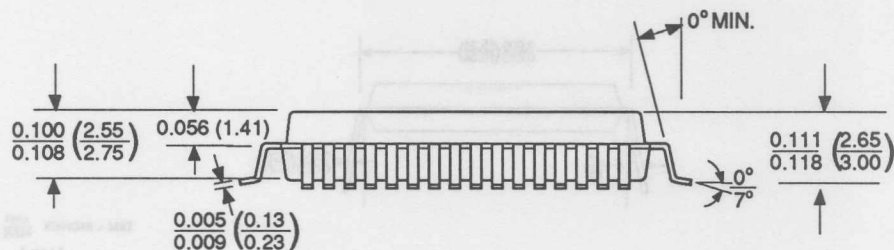
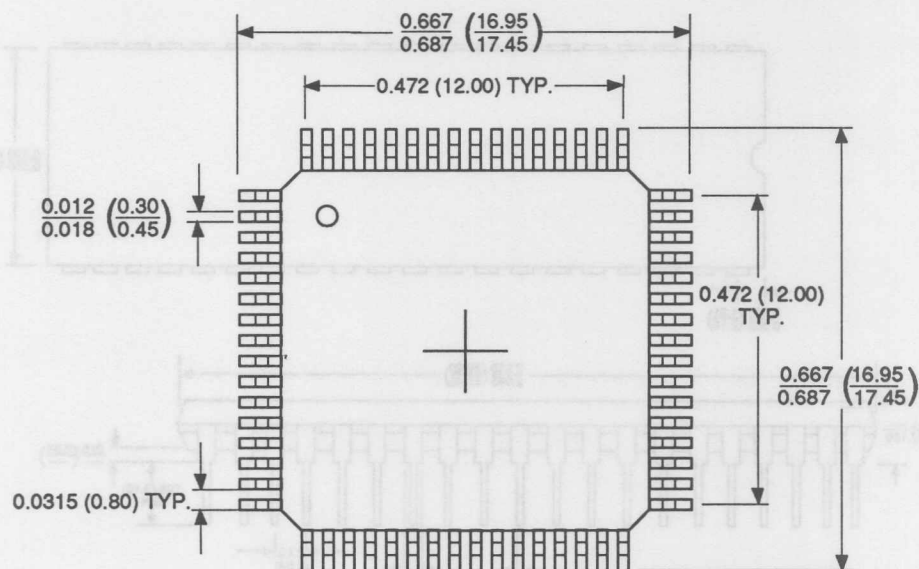


DIM - INCHES MIN MAX
DIM - mm (MIN MAX)



Quad Flat Pack 64 pin

64 - QFP



DIM = INCHES $\frac{\text{MIN}}{\text{MAX}}$

DIM = mm $\left(\frac{\text{MIN}}{\text{MAX}} \right)$

Product Quality and Reliability 8



RELIABILITY OVERVIEW

At Simtek we take a number of complementary approaches to assure the reliability of our products.

First, we develop monitoring devices on product wafers (either as separate chips on the wafer or in the "streets" between the rows of die on the wafer) which help characterize various key elements of the product during the design and process development stages.

As part of the development process we start taking devices through detailed characterization lifetest well beyond data sheet to ensure that there are no functional or reliability weaknesses in the design or manufacturing process technology. Any problems we find are analyzed and their solution fed directly back into the design or process.

We then establish statistically-derived acceptance limits on the parametrical performance of these devices so that each production lot built may be evaluated for conformance before being shipped to assembly. This approach links directly to Statistical Process Controls put in place to ensure that the product built and shipped to our customer base is consistent in its quality and reliability performance. Any trends away from a statistically controlled state are detected early and corrected before they become a problem to our customers.

Before a product is released to the market, we subject samples to numerous long-term life tests which are described in detail in a later section of this document. Qualification testing includes a rigorous characterization of the product against data sheet over the full range of permitted operating conditions. These tests are intended to evaluate performance against data sheet over extended periods of time and under extreme operating conditions, to ensure that our products meet, at a minimum, the industry standard levels of reliability. From there on we continue to take whatever measures are necessary to improve that performance. Our approach on all quality and reliability issues is always to improve on our current performance.

Finally, once the product is released to the market place, we establish a comprehensive monitoring program which allows us to ensure that at a minimum we maintain existing levels of quality and reliability. Analysis of failures from the program provides an opportunity to put in place corrective actions which result in improvements to our product range over time.

AN INTRODUCTION TO RELIABILITY CONCEPTS

One of the fundamental concepts in reliability is the "Bathtub" curve, as illustrated in Figure 1. This describes the relationship between failure rate and time for a well behaved product. It shows the early life "infant mortality" failure rate being relatively high, but moving quickly to a long period of "Random Failures" at a very low failure rate. We then see the failure rate beginning to increase once more, first gradually then sharply, as the product reaches the end of its life (the "Wearout" phase). Time is plotted against a logarithmic scale, since the period of normal lifetime performance is usually very long in relation to the end effects, and is typically much longer than the expected lifetime of most systems that the components are in.

It is the supplier's task to eliminate the product "Infant Mortality" before releasing the product to the customer. This is done using environmental and electrical screens in the product assembly and final test flows.

The useful lifetime failure rate, which is the failure rate that the customer will experience in the field should be at a very low level, and stable, over the required lifetime of the part. The actual failure rate will depend on many variables, including the environmental conditions the devices are exposed to, the actual system operating conditions and the frequency of use.

These different parts of the reliability curve derive from what is happening in the device itself. Failure mechanisms during the infant mortality part of the curve may arise from random defects built into the product during the manufacturing process. Well established examples are defects related to oxide layers, contamination, metal lines and vertical contacts, die attach, wire bond and lid seal. Typical useful life failure mechanisms will relate to such problems as mobile ionic contamination, residual oxide defects, bulk silicon defects, soft error and charge loss mechanisms. The device wearout will generally be attributable to charge loss, hot carrier effects, electromigration, oxide wearout, intermetallic corrosion, and metallic grain growth. The majority of failure mechanisms occurring in semiconductor memory products have been well characterized, and the time to failure will almost always be a function of either temperature, or applied voltage, or both.

Since the majority of manufacturing defects are quickly accelerated by temperature, it is possible to screen out infant mortality by using traditional environmental screening techniques such as biased burn-in and electrical test at temperature and voltage extremes.

The temperature/time relationship for a wide range of failure mechanisms is described by the Arrhenius equation:

The temperature/time relationship for a wide range of failure mechanisms is described by the Arrhenius equation:

$$A_F = \exp\left(\frac{E_a}{k} \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

Where: E_a is the Activation Energy for the failure mechanism measured in electron Volts
 T_1 is the Rated Operating Temperature in °K
 T_2 is the Accelerated Test Temperature in °K
 A_F is the Acceleration Factor for temperature T_2 in relation to T_1
 k is Boltzmann's constant.

This relationship enables suppliers to subject products to accelerated test conditions over a relatively short period of time in order to simulate the lifetime performance of the product and relate the results back to normal operating conditions with a high level of confidence.

Accelerated life testing thus enables us to determine both the product lifetime failure rate due to random failures, and the particular failure mechanisms which predominate through the lifetime of the product. In this way, corrective action may be taken in either tightened screening procedures or modifications to the design or manufacturing process in order to reduce the incidence of failures.

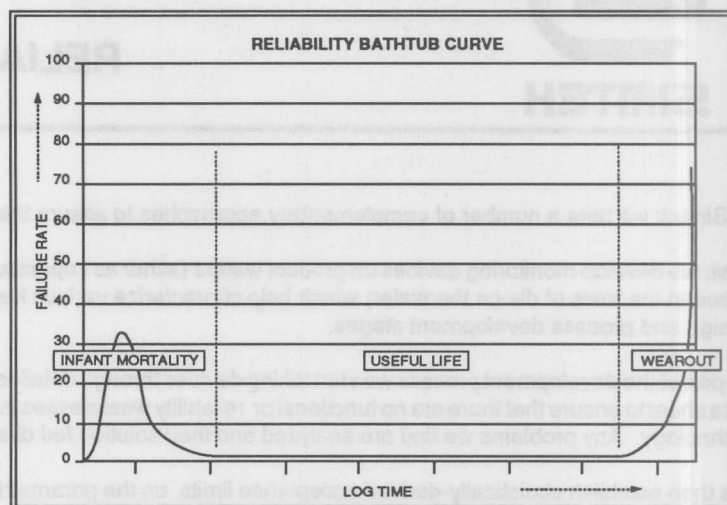


Figure 1. Typical "Bathtub" Curve showing the relationship between Failure Rate & Product Lifetime.

The lifetime failure rate is generally measured in FITs. One FIT is one failure in 10^9 device hours. Thus a failure rate of 100 FITs, for example, would represent a probability of experiencing one failure in 10^7 device hours, or one failure in about 1,150 years. Among the numerous variables that may affect the application of FIT rate data are the confidence level at which the failure rate is calculated (FIT rate calculations are generally based on samples from a larger population, and the confidence level applied to the calculation may typically range between 50% and 95%), the temperature at which the failure rate is calculated (the number of device hours is a function of the acceleration factor applied to the FIT rate calculation), and the number of devices in the system under review.

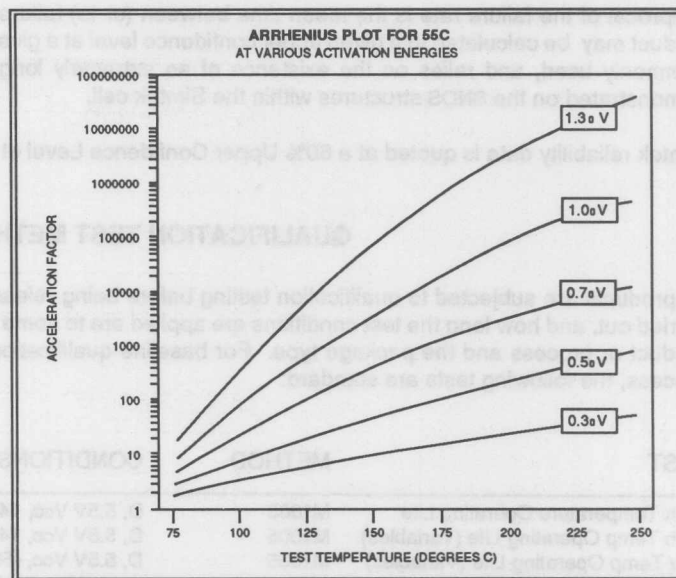


Figure 2. 55° C Data: Acceleration Factor vs. Accelerated Test Temperatures ranging from 75° C through 250° C for selected Activation Energies

METHODS FOR DETERMINING FAILURE RATES

The methods used by Simtek for determining failure rates are industry standard.

CMOSSRAM failure rates are derived from High Temperature Operating Life data. Depending on the actual failure mechanisms observed, the failure rate will be calculated based on the following:

$$\lambda_{(CMOS)} = \left(\frac{\left(\frac{(Total\ Failures)(\chi^2/2)}{(Device\ Hours\ @\ Rated\ Temp)} \right)}{\left(\frac{(Total\ Failures)(\chi^2/2)}{(Device\ Hours\ @\ Rated\ Temp)} \right)} \right) \times 10^9\ FITs$$

Where $\lambda_{(CMOS)}$	is the CMOS failure rate in FITs
1 FIT	is one failure in 10^9 device hours at the rated temperature
$(\chi^2/2)$	is the statistical weighting applied in relation to the sample size at a given upper confidence limit
Device Hours	is the (total number of devices) x (acceleration factor for T_2 in relation to the rated temperature T_1) x (total test hours at test temperature)

Retention failure rates are based on Retention Life data, using samples already cycled to end of data sheet endurance life. A failure in retention is defined as the inability to recall the originally stored data in one or more cells in the array. The Activation Energy applied to recall failures resulting from Retention Life testing is 0.6eV. This value has been derived empirically from single cell and product level analysis using the two temperature method to determine differential decay rates. Simtek Retention Reliability data is based on fully cycled devices.

Simtek uses the normal methodology for deriving the product retention specification at temperature. The failure rate (in FITs) over the random failure lifetime of the part is derived from product retention monitor data. The

reciprocal of the failure rate is the mean time between (or to) failure. Thus the retention specification of the product may be calculated to a given upper confidence level at a given operating temperature. This method is commonly used, and relies on the existence of an extremely long intrinsic cell retention. This has been demonstrated on the SNOS structures within the Simtek cell.

Simtek reliability data is quoted at a 60% Upper Confidence Level at 55°C, unless otherwise indicated.

QUALIFICATION TEST METHODS

All products are subjected to qualification testing before being released to the market place. What tests are carried out, and how long the test conditions are applied are to some extent a function of the "newness" of the product or process and the package type. For baseline qualification of a new design and/or manufacturing process, the following tests are standard:

TEST	METHOD	CONDITIONS	DURATION
High Temperature Operating Life	M1005	D, 5.5V V _{cc} , 140°C	1000 hrs.
High Temp Operating Life (Variables)	M1005	D, 5.5V V _{cc} , 140°C	1000 hrs.
Low Temp Operating Life (Variables)	M1005	D, 5.5V V _{cc} , -55°C	1000 hrs.
Temperature Cycle	M1010	C, -65°C to + 150°C	1000 cycles
Endurance Life	M1033	Room ambient	End of Life (datasheet)
Retention Life	M1008	Unbiased, 150°C (min)	1000 hrs.
Autoclave (PCT)	JEDEC 22-B A102	121°C, 2 ATM, 100% RH	168 hrs.
Temperature, Humidity, Bias (THB)	JEDEC 22-B A101	85°C, 85% RH, 5.0V V _{cc}	1000 hrs.

Table 1: Typical product qualification test methods and conditions.

This series of tests was designed to assess the reliability of the SRAM memory array and peripheral 5.0V circuitry and of the NV array and related high voltage circuitry including charge pumps on the product. Test methods and conditions employed are industry standard, based on MIL-STD-883 and/or JEDEC 22. Testing will generally be continued beyond the stated test duration in order to evaluate device wear-out failure mechanisms.

A more detailed description of the purpose and conditions of each test method is given in the following paragraphs. See *Figures 3* and *4* for the Qualification Flows.

High Temperature Operating Life (HTOL)

This test is essentially a prolonged burn-in under dynamic stress conditions. Transistors in the memory array are continuously toggled on and off over the period of the test under loose timing conditions, under a V_{cc} max condition of 5.5V. It is carried out at a highly accelerating temperature of 140°C, thus ensuring that the 1,000 hour data represents a substantial operating lifetime (in this case, against a nominal E_a of 0.7eV, 1,000 hours would represent the equivalent of approximately 18.5 years at 55°C).

HTOL is a well established lifetesting method for identifying failure mechanisms related to contamination, metal and oxide defects. It will also show up parametric drift over time (e.g., access time push-out).

High Temperature Operating Life (HTOL), Variables Data Collection

A sample of serialized units is subjected to HTOL testing. Rather than base results on go/no go endpoint testing as in the standard HTOL test, the major groups of AC, DC and NV parameters are measured at each read point, including the zero hour. The data is analyzed and variations between read points on each parameter are reviewed. Any variation greater than five percent of nominal is carefully reviewed. The test is looking for parametric drift over time, under worst case operating conditions.

Low Temperature Operating Life (LTOL), Variables Data Collection

Units are placed on a low temperature dynamic lifestest in order to evaluate hot carrier effects that can severely impact device stability and performance on products which use small geometry technologies (generally 1 micron feature size or less). A five percent or greater shift is regarded as significant over a 1,000 hour period. The test is essentially the same as HTOL, but is carried out at low temperature. Variables data is collected from the serialized parts at each read point.

Temperature Cycle (T/C)

This test cycles the units relatively quickly between temperature extremes (-65°C to $+150^{\circ}\text{C}$), thus simulating the thermal stresses which affect the devices when in system use. Failure mechanisms related to die bond, wire bond, package seal and substrate cracking will be exercised by Temperature Cycling.

Autoclave (PCT)

The autoclave test is a crude measure of plastic package performance under high moisture conditions. It gives a good first cut measure of package porosity and die passivation integrity under extreme conditions of moisture and pressure. JEDEC 22-B A102 test method is used and a clean result at 168 hrs. is required for qualification.

Temperature, Humidity, Bias (THB)

This test is a somewhat more refined version of autoclave, in which the device is subjected for extended periods to a high temperature and moisture environment under nominal power supply conditions. JEDEC 22-B A101 test method is used through a minimum of 1000 hrs. HAST testing, a highly accelerated form of the THB test which has been well characterized in terms of the test condition acceleration factor, is under review for application to Simtek products.

Lifestest Sample Pre-Conditioning

In a number of cases lifestest samples are put through a pre-conditioning step prior to testing which generates high internal moisture content in the plastic package followed by simulated IR Reflow as typical board component soldering.

Endurance Life

Samples are subjected to full data sheet specification cycling. The objective is to provide a data point for the failure rate attributable to endurance failure mechanisms, and to verify the adequacy of the in-line production screen. The high voltage elements in the NV circuitry are exercised during this test, which will show up weaknesses in the high voltage oxide layers. The nonvolatile array is subjected to a series of endurance cycles, where one cycle is defined as "STORE ONE", "STORE ZERO". Devices are read every thousand cycles to verify that the store operations are being carried out. 100,000 cycles is the standard test. Some samples are subjected to extended cycling through 1,000,000 cycles.

Retention Life

Samples with a data pattern stored in the nonvolatile array are placed on a high temperature, unbiased bake. The parts are then read periodically to determine whether the cells have retained the data stored at the beginning of the test. A failure is defined as a device in which one or more cells fail to recall the originally stored nonvolatile data state. Apart from providing a direct measure of retention lifetime performance, this test will also exercise failure mechanisms relating to metal integrity, chemical corrosion and substrate bulk defectivity.

Datasheet Characterization

A full datasheet AC, DC and NV characterization of the product is carried out over extreme V_{cc} conditions of 4.0 to 6.0 volts, over the temperature range -40°C through $+85^{\circ}\text{C}$. Interim temperature reads are taken at 0°C , 25°C , and 70°C , so that both commercial and industrial operating temperature ranges are supported. The results are reviewed against datasheet to determine marginalities and expected operating margin under varying conditions. "Guaranteed but not tested" specifications are characterized at this time. All of the characterization data is documented.

Product Reliability Overview

TEST NAME	TEST METHOD	TEST CONDITION	SAMPLE SIZE ACCEPT ON (*)
Constant Acceleration	883, 2001	E	25/1
Mechanical Shock	883, 2002	B	25/1
Variable Vibration	883, 2007	A	25/1
Moisture Resistance	883, 1004	-	25/1
Salt Atmosphere	883, 1009	A	25/1
Resistance to Solvents	883, 2015, JEDEC B107	-	5/0
Solderability	883, 2003, JEDEC B102	-	3/0
Seal [Fine Leak]	883, 1014	A	25/1
Seal [Gross Leak]	883, 1014	C	25/1
Bond Strength	883, 2011	D	4/1
Physical Dimensions	883, 2016, JEDEC B100	-	5/0
Lead Integrity	883, 2004	B2	3/0
Adhesion, Lead Finish	883, 2025	-	5/0
Internal Visual/Mechanical	883, 2013	-	5/0
Internal Wafer Vapor Content	883, 1018	-	3/0
Thermal Shock	JEDEC A104	C, -40/+125°C	25/0
Temperature Cycle	JEDEC A106	B, -40/+125°C	25/0

* Sample Size, Accept number (e.g., sample size of 25, accept on zero rejects, reject on one or more rejects)

Table 2: Environmental test method detail for package qualifications.

ESD Characterization

Electrostatic Discharge characterization is carried out on new designs and when a design change is made that is likely to affect ESD performance. The MIL-STD-883 method M3015, "Human Body Model" is used.

Package & Assembly Line Qualifications

The package qualification procedures and environmental test methods used for hermetically sealed packages are those defined in MIL-STD-883, Method 5005, Group D, and JEDEC 22-B for plastic packages. These generally have universal acceptance by material suppliers, assembly lines and product customers.

Package qualifications are carried out on new package configurations, which include basic package type (DIL, CERDIP, LCC, PDIP, SOIC, etc.), on changes in pin count, on changes in material supplier and major change to package component design or manufacturing method, and for changes in assembly site.

MIL-STD-883 PRODUCT QUALIFICATION

Product built in compliance with MIL-STD-883, Class B (Compliant non-JAN, meeting the requirements of MIL-STD-883, para 1.2.1) is screened and qualified to the test methods set out in Methods 5004 and 5005. Simtek currently has three published standard military drawings for its nvSRAM products. The SMD numbers are: 5962-92324, 5962-93056, and 5962-94599.

Die qualification is based on the Group C requirements of MIL-STD-883, Method 5005, plus retention and endurance lifetest qualification test methods.

Package qualification is per Mil-Std-883 Method 5005, Group D.

The qualification schedule for Group C and D is outlined in Figure 4. Periodic conformance testing conforms to MIL-STD-883, para 1.2.1.

PRODUCT MONITORING PROGRAM

A Product Monitoring Program (PMP) is used to provide continuous assessment of Simtek product reliability. The program calls for samples to be taken at regular intervals from completed product (finished goods, i.e., the product which will be shipped to the customer base). The following monitors are run:

- High Temperature Operating Life
- Temperature Cycle
- Endurance Life
- Retention Life
- Temperature/Humidity/Bias (THB)
- Autoclave

The results of the monitors support a cumulative reliability database. Results are made available to Simtek's customer base via periodic Reliability Updates, available through Simtek Sales and Marketing organization.

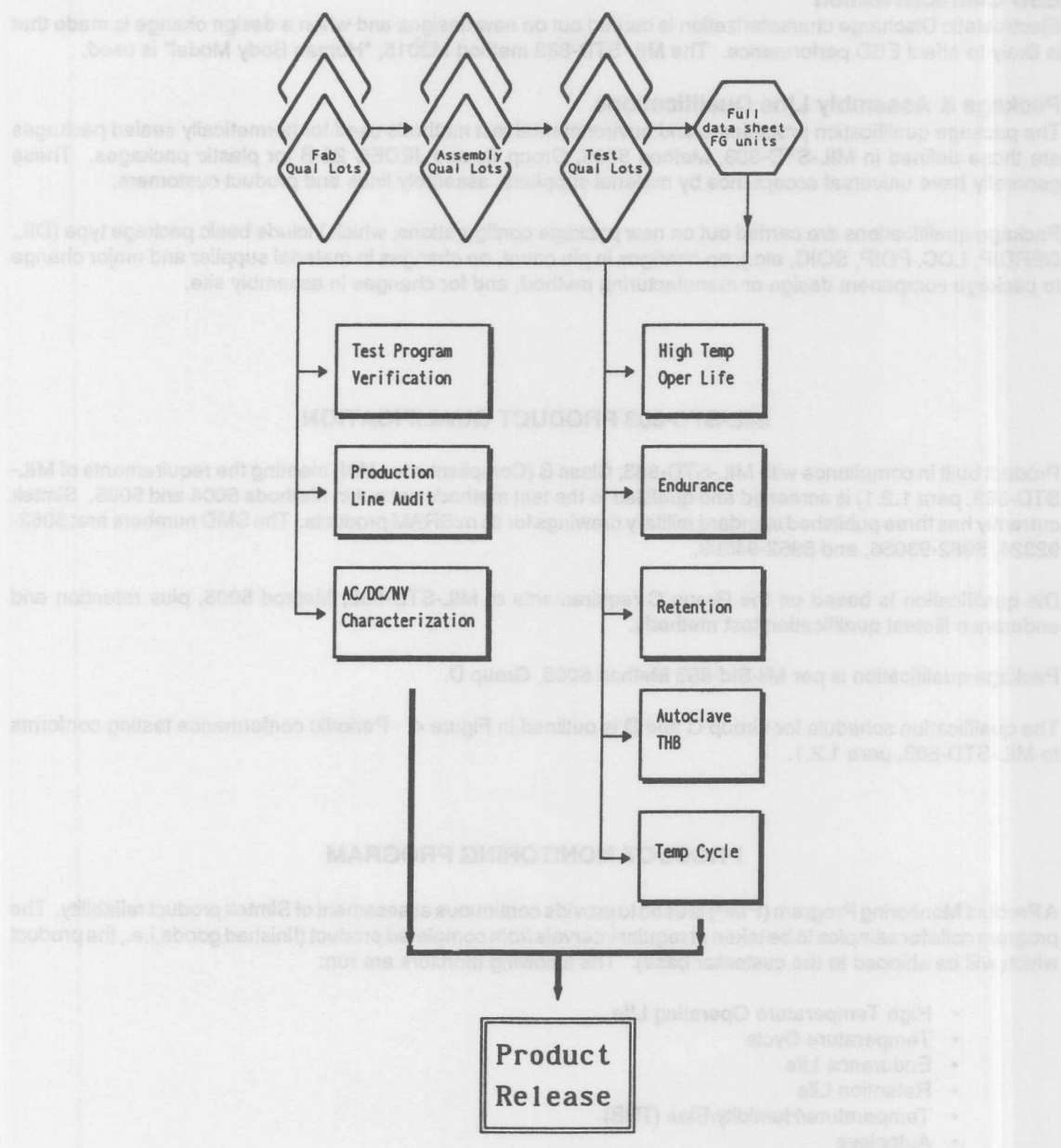


Figure 3: Commercial/Industrial Qualification Test Flows

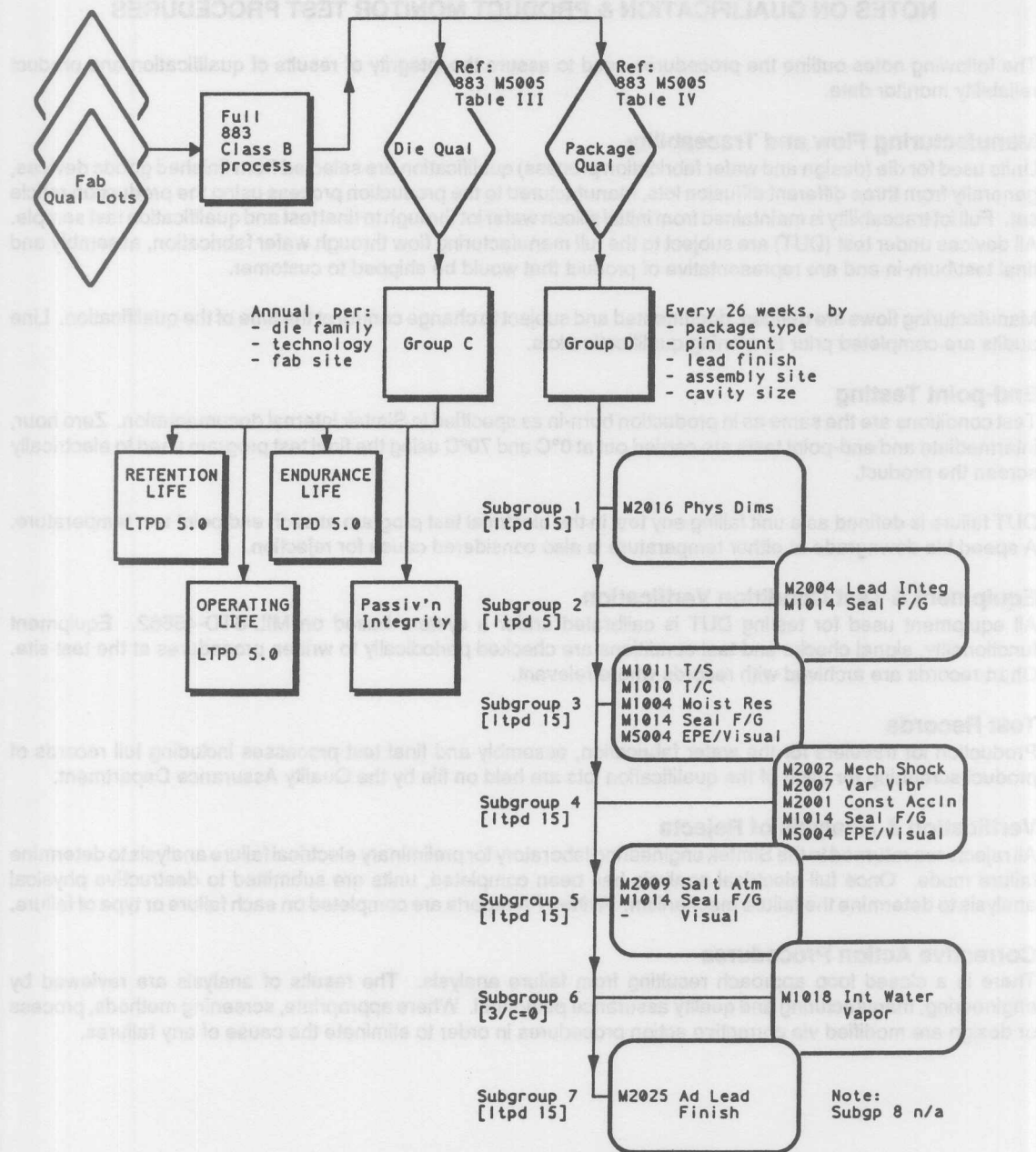


Figure 4: MIL-STD-883 Qualification Test Flows for Class B Product.

NOTES ON QUALIFICATION & PRODUCT MONITOR TEST PROCEDURES

The following notes outline the procedures used to assure the integrity of results of qualification and product reliability monitor data.

Manufacturing Flow and Traceability

Units used for die (design and wafer fabrication process) qualification are selected from finished goods devices, generally from three different diffusion lots, manufactured to the production process using the production reticle set. Full lot traceability is maintained from initial silicon wafer lot through to final test and qualification test sample. All devices under test (DUT) are subject to the full manufacturing flow through wafer fabrication, assembly and final test/burn-in and are representative of product that would be shipped to customer.

Manufacturing flows are defined, documented and subject to change control at the time of the qualification. Line audits are completed prior to running qualification lots.

End-point Testing

Test conditions are the same as in production burn-in as specified in Simtek internal documentation. Zero hour, intermediate and end-point tests are carried out at 0°C and 70°C using the final test program used to electrically screen the product.

DUT failure is defined as a unit failing any test in the electrical test program at each end point test temperature. A speed bin downgrade at either temperature is also considered cause for rejection.

Equipment & Test Condition Verification

All equipment used for testing DUT is calibrated under a system based on MIL-STD-45662. Equipment functionality, signal checks and test conditions are checked periodically to written procedures at the test site. Chart records are archived with records where relevant.

Test Records

Production lot travelers for the wafer fabrication, assembly and final test processes including full records of product screening for each of the qualification lots are held on file by the Quality Assurance Department.

Verification & Analysis of Rejects

All rejects are returned to the Simtek engineering laboratory for preliminary electrical failure analysis to determine failure mode. Once full electrical analysis has been completed, units are submitted to destructive physical analysis to determine the failure mechanism. Written FA reports are completed on each failure or type of failure.

Corrective Action Procedures

There is a closed loop approach resulting from failure analysis. The results of analysis are reviewed by engineering, manufacturing and quality assurance personnel. Where appropriate, screening methods, process or design are modified via corrective action procedures in order to eliminate the cause of any failures.



QUALITY MANUAL

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INTRODUCTION

This manual is intended to answer most of the questions arising in customer's minds about the quality assurance program in place at Simtek. It covers both in-house and subcontracted operations.

An important start point for customer understanding of Simtek as a supplier is where the major components of our product operations are located. Starting at the beginning:

- Our DESIGN group is based at our headquarters in Colorado Springs, Colorado, USA.
- PROCESS DEVELOPMENT is centered in Colorado Springs. We then set up joint development programs with our technology development partners, using their foundry facilities to support development and optimization of our fabrication processes.
- PRODUCT DEVELOPMENT is also based in Colorado Springs, using our own laboratory resources. The Simtek lab functions as the benchmark for product performance. All of our baseline wafer level test structure and product level characterization work is carried out here, as well as the development of wafer and device level electrical test methods and conditions. Thus, the lab equipment and test programs act as reference standards against which our subcontracted test operations are verified.
- MANUFACTURING is 100% subcontracted. Our manufacturing operations are managed from our Colorado Springs base, but each key element in the manufacturing flow - from Mask making through Wafer Fabrication, Wafer Probe, Assembly and Final Test and Speed Sort - is carried out as a subcontracted operation.
- PRODUCT SHIPMENT may be drop shipped direct to the customer from the final test site, or from the Colorado Springs base where Finished Goods Inventory is maintained. This is a function of customer specification for shipment, and experience level of the final test subcontractor.

The currently qualified manufacturing subcontractors, their names and locations, are listed on page 8-17.

QUALITY PROGRAM

This section outlines the main components of the Simtek quality program. More detail of each component is provided in the *Internal Controls* and *Subcon-*

tractors sections.

ISO-9000

The quality system implemented at Simtek is based on the ISO-9000 standards. Chartered Semiconductor Manufacturing and Anam are both certified to ISO-9002. EPI Technologies is certified to the equivalent level under a Texas Instruments sponsored program.

Commercial and Military Programs

Simtek supplies both commercial and industrial grade product, and product compliant with MIL-STD-883 (Class B, Compliant non-JAN). In addition, we offer a number of products under the US Defense Electronics Supply Center (DESC) Standardized Military Drawing (SMD) program. As a result, we support two nominally separate quality program plans - the Mil-I-45208 Inspection System and Mil-I-38535 Appendix A Quality Program Plan for our military product lines, and our ISO-9000 based quality program plan for non-military product lines. In practice the two share many key features, and differ only in some detail. The main differences between the product lines are in the production flows and screening details.

Quality Program Plan Components

The key components of the quality program plan are as follows:

Specifications:

- Documentation control for design, process, test, acceptance criteria and materials specifications;
- Materials procurement control;
- Test Software control;

Records:

- Records archive, including production, test and inspection records;

Subcontracted Services:

- Subcontractor control via subcontractor quality program plan;

Failure Analysis:

- Failure analysis procedures for the identification of failure mechanisms, their cause in relation to the manufacturing process, and corrective action procedures;

Customer Drawing/Specifications:

- Review and control of customer specifications;
- Major change notification;

Internal Audit:

- Internal audit function;
- Internal Quality Indices;

Process Control:

- Statistical Process Control and the minimization of process variation;
- Product Characterization;
- Product Quality Indices

Product Quality & Reliability Measures:

- Qualification Program
- Product Monitoring Program
- Outgoing Defect Rate in PPM

Statistical Process Control

The key to Simtek product assurance is the use of statistical methods in establishing and maintaining control in the manufacturing process. Since all of our manufacturing is subcontracted, we work closely with our suppliers in developing, implementing and monitoring SPC on the production lines. This includes establishing specifications (target, max and min), carrying out process capability studies to determine initial C_{pk} values⁽¹⁾, identifying critical parameters, and using process control charts to monitor the process. Control is generally established through the manufacturing

equipment, and measures taken on that equipment.

Other Statistical Tools

Numerous other statistical tools are used to support engineering work on the process and the products. Process Development studies rely heavily on the use of Experimental Design (DOE) techniques. Yield analysis, failure analysis and characterization work all make use of in-house tools such as RS1. Off-line analysis of subcontractor outgoing quality uses PC-based SQC tools.

Simtek Quality Indices

We are in the process of defining a number of performance measures which we believe will be very high on our customer's list of concerns. These measures will cover outgoing product quality, reliability and service to the customer base. Performance targets are set through 1994. In addition, we have defined a series of measures by which we judge the performance of our subcontractors and material suppliers. Now that we have completed basic product and line qualifications and have begun to increase production volumes, we will be adding customer service measures such as on-time delivery and failure analysis response time to the list in the near future.

Index Definitions:

Performance	Units of Measure	Definition & Source of Data
Outgoing Electrical Defect Rate	Parts per Million (PPM)	Rolling 3 month average in ppm, measured at the QA Electrical Gate per JEDEC-16, EIA-554. See <i>Customer Support</i> section for discussion of calculation method.
CMOS Failure Rate	FITs ⁽²⁾	Cumulative FIT rate resulting from High Temperature Operating Life testing in qualifications and product monitors.
Retention Failure Rate	FITs	Cumulative FIT rate resulting from Long Term Retention bakes in qualifications and product monitors.
Endurance Failure Rate	Percent failing at end of data sheet life	Cumulative failure rate resulting from 10 ⁴ endurance cycle testing in qualifications and product monitors. 10 ⁵ endurance cycle data will be added in the near future.

¹ a C_{pk} value of at least 1.3 is regarded as satisfactory - any critical parameters with lower C_{pk} values are subject to a corrective action program.

² Where 1 FIT is 1 failure in 10⁹ device hours at nominal operating temperature. Failure rate calculations use a 60% upper confidence limit unless otherwise stated.

INDEX	1993 Act.	1994 Act.	1995 Target
Outgoing Electrical Defect Rate (ppm)	65	50	<50
CMOS Failure Rate (FITs) ³	30	26	<25
Retention Failure Rate (FITs)	5	<5	<5
Endurance Failure Rate (%)	0.25%	0.12%	<0.1%

Subcontractor

The following indices have been developed as measures of subcontractor/supplier performance. These measures are in the process of being implemented on all qualified subcontractors.

WAFER FOUNDRY FUNCTION INDICES:

- Critical Process Step Control indicators - as C_{pk} . An outline of critical wafer fabrication is given in *Table 1*.
- Yield
- Cycle Time
- Non-Conformance Rate
- Unit Processing Cost

ASSEMBLY

FUNCTION INDICES:

- Process Step Control Indicators (Bond Strength, Die Shear, Hermeticity) - C_{pk}
- Yield
- Cycle Time
- Non-Conformance Rate
- Unit Processing Cost

PACKAGED PRODUCTION FINAL TEST

FUNCTION INDICES:

- Lot Reject Rate @ Electrical & Visual QA Gates
- Electrical Outgoing PPM
- Visual Outgoing PM
- Cycle Time
- Non-Conforming Rate
- Unit processing Cost

MATERIALS SUPPLIERS

FUNCTION INDICES:

- Lot Reject Rate @ Incoming
- On time delivery
- Lead time
- Unit cost

³ Please see the "Reliability Overview" section, and Simtek publication 05-32-003 for more detail on reliability measures and current data.

Typical critical process step indicators chosen to provide visibility of the stability of the wafer fabrication process are listed in *Table 1*. Reports are provided by the foundry. The data used to track these indicators is drawn direct from the foundry engineering data collection system, and is directly available to the foundry engineering team. Month to month performance is a subject for discussion at regular Simtek/Foundry performance review meetings.

STEP	MEASURE
Critical Dimensions	Active, Poly, Metal
Oxide Thickness	Low & High Voltage, Gate, Sidewall, Field
Memory Nitride	Refractive Index
Memory Nitride	Thickness
Poly	Thickness
LTO	Etch Rate
LTO	Thickness
Defect Counts	at Critical Layers
Memory Cell	Parameters

Table 1: Process Control Indicators for Wafer Fabrication

INTERNAL CONTROLS

Documentation

All documentation related to the product is under a document control system within Simtek. This system assures that specifications are generated to support product introduction, that they are approved by the right people in Simtek before they are released, and that any changes made to the documents are also scrutinized and approved before release. The documentation system also serves Simtek's subcontractors, ensuring that the specifications necessary to support manufacturing are available at the subcontractor's own facility (this is dealt with in more depth under the *Subcontractor* section).

The in-house documentation system covers the following main areas of activity:

- Design
- Manufacturing process

- Raw materials
- Testing - methods, conditions and software
- Characterization
- Data Sheet or Data Book
- Inspection and acceptance criteria.

Design

All of the design work for Simtek products is carried out by Simtek personnel. Internal design review procedures ensure that proposed changes are approved and planned for before work is started on them. Each major design revision is assigned an Alpha revision level. An Alpha revision is defined as a revision that will require both internal and customer re-qualification (for example, a shrink, or major change in functionality on die). Engineering revisions within the major Alpha revision levels are given numeric IDs. These are always minor changes, intended to improve product performance or yield. Simtek marks the top side of its product with the Alpha revision level of the die, and customers are notified well in advance of plans to introduce a new Alpha revision level. The engineering revision level is generally kept internal to Simtek, since controls are in place throughout the manufacturing flow to ensure that such changes do not affect the form, fit or function of the product. In other words, they are a non-issue to the customer.

Process

Simtek works with its technology partners to develop wafer fabrication processes on which to build its products. These are basically conventional CMOS processes with SNOS modules to support the nonvolatile cells in the nvSRAM array. Thus the only arguably novel aspect of the basic process flow is the SNOS module, and this is in fact not particularly novel in itself. SNOS has been used for many years by numerous semiconductor suppliers of nonvolatile memory products.

Having established a process specification, it is then documented and changes to it are controlled as with any other manufacturing specification. We take great care to ensure that process changes do not affect the form, fit or function of the end product. Where we do decide to implement a major process change, those customers specifying change notification in their procurement specifications will be notified in advance of the change. Such changes are rare, and are generally subject to both re-qualification through lifetest procedures, and re-characterization, to ensure that the product data sheet is not violated by the change.

Product Characterization

Our Product Engineering group is responsible, amongst many other things, for ensuring that the product meets data sheet under worst case conditions. We therefore develop characterization routines for our products that test the device over a range of operating conditions extending well beyond the data sheet extremes, using data patterns and test algorithms designed to exercise the device across all parameters. This approach quickly shows up any performance marginalities, which are then addressed by modifying the design or the process. Once the new product completely meets the data sheet, a final characterization sample is run over an extended V_{cc} range (4.0V to 6.0V) and over an extended temperature range (-57°C to +130°C) for all AC and DC parameters.

NV performance is evaluated during the product development phase by running accelerated lifetests on both single cell test structures and on packaged product to ensure that the device meets the data sheet endurance and retention specifications (these tests are described in more detail in the *Product Reliability Overview*).

Product characterizations are routinely performed when any significant process or design changes are implemented (see the above sections on Process and Design for details), and are carried out periodically to ensure that the device has not drifted over time (this is a highly unlikely event, due to the presence of process monitors and parametric acceptance criteria which would detect such changes well before they became significant at the product level).

Engineering Lab

Simtek has established in-house test capability at the wafer and packaged product levels in order to support device characterization and development of production screens. The laboratory also supports electrical failure analysis down to level of single cells in the memory array. The key items of equipment in the Simtek lab include:

- Keithley parametric tester for analysis of street test structures.
- Teradyne J387 tester and bit-map for wafer level functional probe and failure analysis.
- Teradyne J937 tester for software development, packaged product characterization and product failure analysis.
- MOSAID tester for product development and analysis

- Aehr test monitored burn-in oven
- Multiple unbiased bake ovens
- Endurance NV cycling equipment

The above items are the most relevant to package level development and electrical failure analysis. There are numerous other items in the lab to support the development workload. Destructive physical analysis is carried out off-site through numerous subcontracted facilities in the USA.

Lab Equipment Calibration

The equipment in the Simtek engineering laboratory is used for a number of critical measures. These are:

- Design Verification
- Definition of Product Characterization
- Definition of electrical test conditions, methods and pass/fail criteria
- Definition of a "good" and a "bad" device
- Electrical failure analysis
- Reference Standard for remote test sites for all final test software.

The equipment used to make these measurements is calibrated to known reference standards. All critical items of equipment in the laboratory are maintained in calibration based on the MIL-STD-45662 calibration system. Traceability to reference standards is maintained through to the N.I.S.

Test Software

Simtek engineering writes the initial test programs for functional wafer probe and final electrical test, including endurance and retention screening. These programs are developed on in-house test equipment in the Simtek engineering laboratory in Colorado Springs. They are developed as a result of extensive characterization of the product, which includes analysis of the worst case data patterns to be used for each category of test.

The test methods and test conditions are then documented in written specifications which are supplied to the electrical test subcontractor. The methods used for correlation and control between sites are described in detail under section 4.

SUBCONTRACTORS

Quality Program

Since Simtek uses subcontractors for all manufactur-

ing steps, we recognize that the methods used to establish and maintain acceptable quality levels will be of prime concern to our customers.

The basis for subcontractor quality is the Simtek Subcontractor Quality Program specification⁵. This document outlines the quality system the subcontractor is required to have in place to support manufacture of Simtek product. Central to this is the expectation that there will be a system in place to establish and maintain statistical control over processes, and that this data will be shared with Simtek on a regular basis.

In a series of meetings with the selected manufacturing facility, personnel from Simtek Manufacturing, Engineering and Quality Assurance review process flows, manufacturing procedures, engineering disposition procedure, change control procedures and acceptance criteria. Once agreed to, they are documented. A formal facility audit also reviews production control, data reporting and communications controls, and establishes quality indices by which the performance of the subcontractor will be judged on a periodic basis. Where possible, we use the subcontractors established procedures and specifications. Where these do not meet Simtek's needs, we add to the subcontractor's program.

A formal procurement specification is released by Simtek, defining all of the above. Subsequent changes, either by Simtek or by the subcontractor, are subject to approval by both parties before implementation. Procedures are put in place to disposition non-conforming product.

Once the production line has been established, Simtek has responsibility for supplying the subcontractor with material to load the line, for dealing with non-conforming material, and for monitoring and reporting on quality and other issues. The subcontractor has responsibility for running the line as if it were his own product line (which it of course is). This includes responsibility for the quality program. Thus in effect, the subcontractor's quality program, and his quality assurance personnel, act as delegates for the Simtek QA department.

Line Qualification

Each subcontractor is subject to initial site audit by Simtek before production material is released onto the new line. Audits are based on audit checklists, which were developed initially for auditing MIL-STD-883 fa-

⁵ This specification is reproduced in Appendix A.

cilities. They take into account as much as possible of the practical issues affecting product quality, including operator training; the effectiveness of communications between the subcontractor and Simtek in relation to production control and change notification; the disposition of non-conforming material; the availability of specifications to operators and methods of approving and implementing changes.

The following subcontractors are qualified to manufacture Simtek product:

Wafer Fab

Chartered Semiconductor Mfg., Singapore

Assembly

Anam, South Korea and The Philippines
Indy Technologies, Manteca, CA, USA

Final Test

EPI Technologies, Richardson, TX, USA

Product Qualification

In addition to line audit, qualification lots are run through the new subcontracted facility in order to qualify the product. The level of qualification (i.e., the number and duration of lifetest methods applied to the qualification) is reviewed in detail in the *Product Reliability Overview* section.

A new wafer fabrication line requires full die re-qualification comprised of:

- High Temperature Operating Life (CMOS reliability)
- Low Temperature Operating Life (Hot Carrier effects)
- Endurance and Retention Life (Nonvolatile reliability)
- Moisture related Lifetesting (for Plastic packaged products)

A new Assembly facility requires package related lifetesting, including full moisture lifetesting for plastic lines.

A new test facility requires a major electrical test correlation with the Simtek tester and test software to be successfully carried out.

Once qualification is completed, delivery of qualified product is approved. From then on, Simtek maintains close communication with the subcontractor manufacturing, engineering and QA organizations to assure

acceptable performance. Simtek intends to provide a quarterly quality report to each subcontractor, and to hold quarterly operations meetings to review progress and help solve problems.

Customers requiring prior notification of change of manufacturing line will be informed in advance of any change of line, and qualification data supporting the line change will be provided for review.

Wafer Fabrication

The Wafer Fabrication process is by far the most complex element in the manufacturing flow, and is, to the extent outlined in the *Process* section, unique to Simtek. As a result, Simtek has tended to enter into close technology development partnerships with its foundries, rather than more conventional foundry arrangements. This works to the benefit of both parties, and Simtek benefits from the fact that the engineering group in the foundry quickly develops detailed knowledge of the process, and a highly focused interest in reliability and yield improvement.

Once the manufacturing process is accepted, it is documented, and the qualification lots run to that process. Any subsequent change is subject to approval by both Simtek and the Foundry engineering group. Weekly conference calls are held between the two parties to ensure continuity in development and problem-solving programs.

Simtek provides the foundry with a detailed procurement specification, which includes the following elements:

- Technology Design rules
- Wafer level (street) test structure specifications
- Process flow
- Parametric acceptance criteria
- Visual acceptance criteria
- Functional probe specification

Within this specification are more detailed requirements covering the following practical issues:

- Change Control and Change Notification
- Procedures for non-conforming material
- Visual inspection
- Lot Documentation
- Rework
- Statistical Process Control Data
- Reliability Monitors and Data
- Failure Analysis support

PROCESS STEP	TYPE	ITEMS MONITORED	FREQUENCY & SAMPLE PLAN
Saw & Clean	Monitor	Visual Equipment Die Water	4/shift, 25 dice, 5 sites 1/shift 1/shift
Die Bond	Monitor	Visual Mechanical	4/shift, 2 strips 2/shift, 2 units
Epoxy Cure	Monitor	Equipment	1/shift
Wire Bond	Monitor	Visual Equipment Mech (Pull test) Ball shear test	4/shift, 2 strips 1/shift 2/shift, 10 wire/2 units 1/day, 5 ball/1 unit
Internal Visual	Lot Acceptance	Visual	LTPD 5.0
Mold	Monitor	Visual Equipment Mech (X-Ray)	4/shift 1/shift 2/shift, 1/4 shot
Post Mold Cure	Monitor	Equipment	1/shift
Mech Deflash/Trim	Monitor	Visual	4/shift, 2 strips
Chemical Deflash	Monitor	Equipment	1/shift
Solder Plating	Monitor	Visual Equipment	1/bath/shift, 116 units 1/shift
Lead Finish	Lot Acceptance	Visual Plating thck Sold (1 hr St Age)	LTPD 2.0 5 units/lot 5 units/lot
PCE Clean	Monitor	Equipment	1/shift
Marking	Monitor	Visual	4/shift, 2 strips
Mark Cure	Monitor	Equipment Oven temp	1/shift 1/shift
Mark Perm	Monitor	Freon TMC	2/shift, 5 units
Trim	Monitor	Visual	4/shift, 2 strips
Form	Monitor	Visual	4/shift, 2 strips
Final Outgoing	Lot Acceptance	Visual	LTPD 2.0
Pack	Monitor	Visual	1/shipment, 3 boxes

Table 2: Assembly Flow Monitors (Plastic Products)

Simtek arranges access to lot data both in-line and end-of-line, so that process step performance as well as parametric and functional probe data may be monitored and analyzed. Reliability monitor data at the wafer level is also supplied on a routine basis.

Assembly

Simtek assembly is currently based at Anam, South Korea, for all plastic products, and at Indy Technologies, California, for all ceramic package types, including the MIL-STD-883 Class B and SMD Class M product lines.

Since the subcontracting of assembly is routine for the semiconductor industry, there is little to add here except to stress that Simtek has selected assembly houses that have a great deal of experience and proven manufacturing quality.

Final Test

Simtek has extensive experience working with final test subcontractors to assure the continuing electrical quality of its finished product. A great deal of effort is invested in establishing effective electrical test methods to assure the functionality of the product over the full operating range⁶.

Once the test procedures have been established, they are transferred to the tester technology at the final test subcontractor. The test subcontractor is responsible for implementing the software on its own in-house testers. Simtek product and test engineering work closely with the subcontractor during this phase. Implementation is finalized with a controlled device correlation between sites, using both good and bad units. The tester and tester correlation includes running detailed device characterizations to ensure all parameters tested correspond over the full temperature range of testing. Test program changes are implemented using similar controls.

Simtek maintains reference units at each test site for test equipment set-up purposes. Production runs are not started until test set-ups have passed calibration and reference unit tests. An ongoing correlation program between the Simtek Lab (the reference standard) and subcontracted test site(s) ensures site to site correlation.

Non-conformances are reviewed on a periodic basis and the pareto chart of causes discussed within Simtek and with the subcontractor. In this way we work

towards elimination of causes of non-conformance and overall improvement of product quality.

Final test data gathered at the subcontractor site is available electronically to Simtek engineering. Test programs routinely collect characterization data of key parameters on a sample basis, thus providing an ongoing measure of product variability over time.

Controlled manufacturing flows are set up by the subcontractor to reflect Simtek requirements. The travelers are approved by Simtek before production begins, and any change to the flow is approved by both Simtek and the subcontractor before being implemented on production material.

CUSTOMER SUPPORT

Quality Data

The outgoing electrical and mechanical quality of Simtek product is measured at quality assurance gates set at the end of the final test process flow. Each final inspection lot is sampled electrically at operating temperature extremes, and a sample is taken for visual/mechanical inspection. These data are used to calculate the probable outgoing defect rate in parts per million.

The measures are referred to as Average Incoming Quality (AIQ) and Average Outgoing Quality (AOQ), and refer specifically in this context to quality measurements within the Simtek test flow. We measure the defect rate after completion of the 100% manufacturing screens (AIQ) and then the defect rate of the product after completion of sampling and rescreening for failed samples (AOQ). Both are measured in parts per million (ppm). We use JEDEC-16 and EIA-554 methods for calculating the defect rates.

The AIQ is the product of:
 (Sample % defective)
 (lot acceptance rate)
 (10⁶)

The AOQ is the product of:
 (Total population - total samples used) / (Total population) [(N-n)/(N)]
 (Estimated population percent defective (from AIQ)) [P]
 (Probability of lot acceptance from the OC curve for the sample plan) [P₂]
 (10⁶)

⁶ See "Test Software", page 8-16.

PROCESS STEP	TYPE	ITEMS MONITORED	FREQUENCY & SAMPLE PLAN
Incoming Inspection	Lot Acceptance	Part Count Gross Visual Traceability	Each lot, 100% Each lot, 100% Each lot
Electrical Test Insert	Monitor Lot Acceptance Lot Acceptance Lot Acceptance Lot Acceptance	Calibration Reference Units Program ID Insert ID Trigger Yield	Each lot 5 per set-up Each lot Each lot Each lot, per insert
Endurance [wafer level screen]	Monitor	Calibration Program ID	Each lot Each lot
Retention [wafer level screen]	Monitor	Calibration Oven Temp	Each lot Each lot
Burn-In	Monitor	Board Cal Board Check Oven Cal Oven Temp	Each board Each board, 5 sockets Each lot Each lot
Burn-In PDA	Lot Acceptance	PDA Calc 2nd submission	Each lot, PDA = 5% PDA = 3%
Topside Mark	Monitor	Mark Content Datecode Tracecode	Each lot Each lot Each lot
Mark Permanency	Monitor	Mark Perm	1 unit, C = 0
Solderability	Monitor	Solderability	3 units, 38 leads, C = 1
Pack	Lot Acceptance	C of C Part Count Rails visual Rails orientation Traceability Electrical verification	Each lot Skip lot sample

Table 3: Test Flow Monitors

Reliability Data

The reliability data derived from qualifications and product monitors is used to generate failure rate reports on a quarterly basis. Details of the Reliability Program at Simtek are in the Data Book. Tabulated reliability data is updated periodically and available via Simtek Marketing.

Specification/Drawing Review

Customers with special requirements, whether they are product specifications outside of Simtek data sheet, or general quality and reliability procurement specifications with detailed test and AQL criteria, should submit detailed drawings via Simtek marketing before placing a purchase order for the product. Simtek has a customer drawing review procedure which ensures that special requirements are reviewed internally by the right people before the company commits to shipping the product. Once approved, special requirements are translated into special processing instructions for the manufacturing sites.

Customer Audit of Simtek Facilities

Simtek welcomes customer interest in its subcontracted manufacturing facilities. Details of control procedures in each of the facilities may be provided in summary form to customers requiring such information, and are generally handled via paper site survey questionnaires. Where a site audit is necessary, Simtek requires at minimum 6 weeks notice so that the subcontractor may have the opportunity to schedule the audit in their facility. Requests for site survey and site audit should be addressed initially through the Simtek Sales and Marketing organization.

Change Notification

Where specified by the customer, advance notification of intent by Simtek to implement major process or design changes will be given through the Simtek change notification procedure. It should be understood that Simtek can only make this commitment to customers who have specifically requested this service.

Failure Analysis on Defective Product

In the event a Simtek customer comes across a technical or quality problem with Simtek product, the Return Material Authorization (RMA) procedure should be followed. Customers should obtain an RMA number from Simtek via the Sales and Marketing organization before returning product. However, this should not delay opening up communications with Simtek in order to start dealing with the problem. Simtek QA and Engineering groups place a high priority on supporting customer problems, and we hope that in the unlikely event you encounter a problem with our product, you will find that we respond quickly and efficiently to resolve the problem.

It is important that we understand what the problem is, and under what circumstances the problem occurs. Once we have the device(s) back (assuming an electrical problem with the part(s)), we immediately put them through full electrical test to assure data sheet functionality. If this does not show up the problem, further analysis is carried out under the application conditions.

This initial phase of verification should take two to three working days. We then get back in contact with the customer to confirm our findings, and review the direction the analysis should take from there on. It is our experience that the vast majority of problems can be dealt with within this three day period based on electrical verification and analysis of the defective units. Where further destructive physical analysis is required, we will generally agree with the customer how long this will take, and set up a reporting structure to keep the customer informed of progress.

Where corrective actions prove necessary as a result of FA, we will generally agree to these in discussion with the customer. At the same time, we will be reviewing what actions we need to take internally to prevent recurrence of the problem.

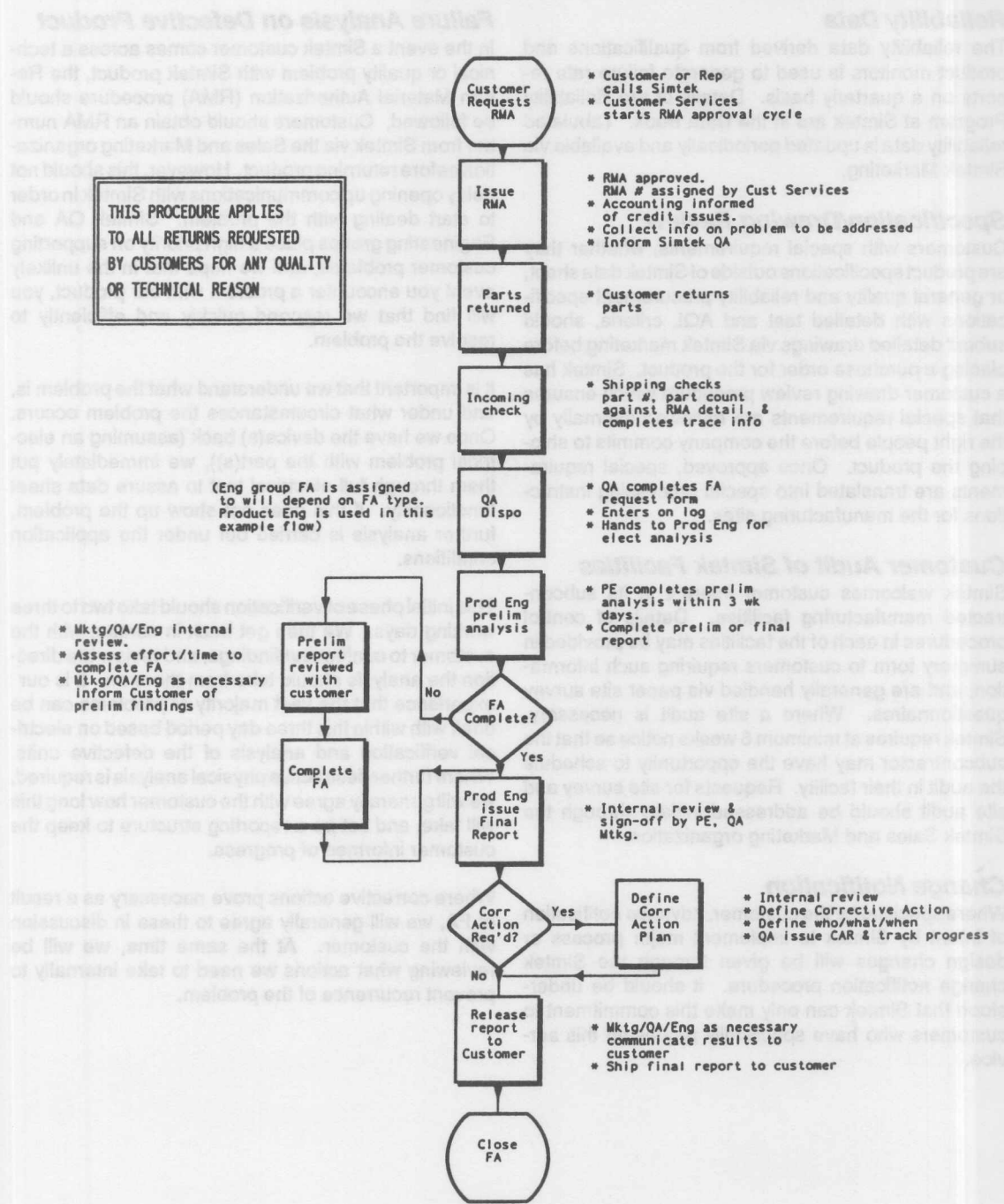


Chart 1: Failure Analysis Flow